

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0323

Roll No.

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B.Tech.

Third Semester Theory Examination, 2011-12

DIGITAL ELECTRONICS

Time : 3 Hours]

[Total Marks : 100

Note : This question paper contains three Sections. Attempt questions from each Section.

Section A

Attempt *all* parts of this question. Each question carries equal marks. 2×10=20

1. (a) Distinguish between weighted binary code and unweighted binary code.
- (b) Convert the Gray code 111001 into binary code. Also draw its logic circuit.
- (c) Write the characteristic equation of J-K flip-flop.

(d) Choose the correct statement :

In a D flip-flop D stands for :-

- (i) Data
- (ii) Dominant input
- (iii) Dual input
- (iv) None.

(e) How many address lines and input-output data line are required for memory unit $8K \times 8$?

- (f) (i) ROMS are volatile or non-volatile ?
- (ii) Is DRAM is slower than SRAM ?

(g) How race can be avoided ?

(h) Draw the logic diagram of Up-Down counter.

(i) Where EX-OR function are used in Electronic circuit ?

(j) Define Cyclic code. Is Gray code a Cyclic code ?

Section-B

Attempt *all* parts of this question.

6×5=30

2. (a) (i) Represent -9 in three different ways.
- (ii) Add two unsigned BCD number 184 and 576.
- (iii) Define Linear Block code. Is 1011, 1000, 1101, a Linear Block code?
- (b) (i) Explain Hamming weight and Hamming distance.
- (ii) What is relation between Hamming distance and Number of corrected bit error?
- (iii) Find the complement of function :
- $$F(A,B,C) = (1,4,5,7).$$
- (iv) Express the Boolean function $F=A+B'C$ as a sum of minterms.
- (c) (i) Simplify the Boolean function :
- $$F(X,Y,Z) = (3,4,6,7)$$
- using K-map.

- (ii) Why NAND and NOR are called universal gate?
- (iii) Distinguish between MEALY and MOORE models.
- (d) Define prime implicants and essential prime implicants.

Find the prime implicant of the given function :

$$F(A, B, C, D) = (2, 6, 7, 8, 9, 10).$$

- (e) (i) Define registers. Write the name of different types of registers. Construct 4-bit parallel shift register and explain it.
- (ii) Write two merits/demerits of synchronous sequential circuit over asynchronous sequential circuit.

Section-C

Attempt *all* questions.

10×5=50

3. (a) Convert BCD code to Excess 3 code.
(b) Draw the logic diagram of CLA generator.

Or

- (a) Construct full adder using half adder. Also write sum and carry.
(b) Draw block diagram of 4-bit subtractor.

4. Attempt any one of the following :

- (a) In a magnitude comparator let $A = A_3 A_2 A_1 A_0$ and $B = B_3 B_2 B_1 B_0$ are two numbers. Draw the expression $A > B$ and $A < B$. Also draw its logic diagram.
(b) Design a code converter that convert a from the 8, 4, -2, -1 code to BCD code.

5. (a) Using K-map draw the circuit diagram of 4 to 1 line multiplexer.
- (b) Distinguish between latch and flip-flops. Draw the logic diagram of D latch. What is the role of preset and clear input of flip-flop?

Or

There are A and B two flip-flop. Whose state equation and output equation are given as :

$$A(t+1) = Ax + Bx$$

$$B(t+1) = A'x$$

$$Y = Ax' + Bx'$$

where x is the input. Draw its state diagram.

6. Attempt any one of the following :

- (a) Assume that the exclusive-OR gate has a propagation delay of 10ns and that the AND or OR have a propagation delay of 5ns. What is the total propagation delay time in the four bit adder?

- (b) Design combinational circuit that generate the 9's complement and 10's complement of BCD digit.

7. (a) Design a four bit binary synchronous counter with T flip-flop.
- (b) Differentiate between PAL and PLA.

Or

- (a) Write the PLA programmable table for BCD to Excess 3 codes.
- (b) A memory size $4K \times 8$ ROM is expanded to $8K \times 8$. Find the number of chips required and the number of address lines in the expanded memory.