Printed Pages : 3 TEC101

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3033 Roll No.

B.Tech

(SEM I) ODD SEMESTER THEORY EXAMINATION 2009-10

ELECTRONICS ENGINEERING

Time : 3 Hours] *[Total Marks : 100*

Note : *Attempt all the questions.*

1 Attempt any **two** parts of the following : **10×2=20**

(a) With a neat energy band diagram, explain the working of a p-n junction diode in reverse bias.

(b) Draw the forward characteristics of a p-n junction diode and explain its :

(i) static resistance

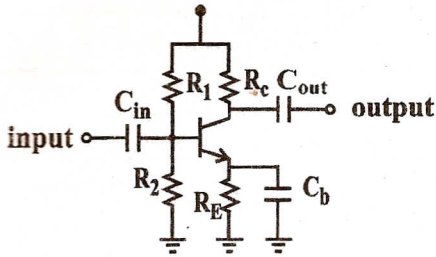
(ii) dynamic resistance and

(iii) average a.c. resistance.

(c) Name the capacitances associated with a p-n junction diode and explain the causes and dependence of these capacitances.

2 Attempt any **two** parts of the following : **10×2=20**

(a) Explain the working of following circuit :



(b) Draw the circuit of a full wave rectifier. Derive the expression for its ripple factor.

(c) Draw the output waveform of a full wave rectifier and compare its performance with (i) C filter (ii) LC filter.

3 Attempt any **two** parts of the following : **10×2=20**

(a) Draw the BJT circuits for CB, CC and CE configurations. Compare Z_i, Z_o, A_V and A_I for the above configurations.

(b) Draw the circuit of a BJT in CE configuration employing voltage divider biasing. Calculate its stability against I_{CO}.

(c) Using a low frequency hybrid model, calculate A_V and A_I of a 2 stage RC coupled BJT amplifier.

Attempt any **two** parts of the following : **10×2=20**

(a) With a neat sketch, explain the working of an n-channel JFET.

(b) With a neat sketch, explain the working of a p-channel depletion mode MOSFET.

(c) Draw the circuit of a JFET amplifier in all the three configurations. Compare A_V, A_I, Z_i, Z_o for all of them.

Attempt any **two** parts of the following : **10×2=20**

(a) (i) Convert

FE ϕ A_{hex} into Decimal 7650 octal into hex 11010110 binary into octal.

(ii) Draw the circuit of a 2 input EX-OR gate using four 2 input NAND gates.

(b) Minimise the following K-Map :

AB \ CD	00	01	11	10
00			1	
01	1	1	1	
11		1	1	1
10		1		

(c) Draw an op-amp based circuit to give $V_0 = V_1 + V_2 + V_3$.