Printed Pages—7 EEC101

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3301 Roll No. | | | | | | | | | | |

B. Tech.

(SEM. I) THEORY EXAMINATION 2011-12

ELECTRONICS ENGINEERING

Time : 3 Hours *Total Marks : 100*

Note :– All Sections are compulsory

SECTION—A

1. All parts are **compulsory**. All questions carry equal marks : **(10×2=20)**

   (a) **What will happen** on number of free electrons in a semiconductor on increasing temperature ?

   (b) A 4.5 V zener is rated at 1.5 watt. What is the maximum safe current of the zener ?

   (c) What are the PIVs for full wave center tapped transformer and bridge rectifier respectively ?

   (d) What is the biasing condition of base-emitter and collector-base junction in the active region of a CB BJT configuration ?

   (e) **Write down the h-parameters of a bipolar junction transistor.**

   (f) **Write the Shockley's Equation for JFET.**

   (g) Write the types of MOSFET and their two major differences.

(h) Write the input and output resistance of an ideal operational amplifier.

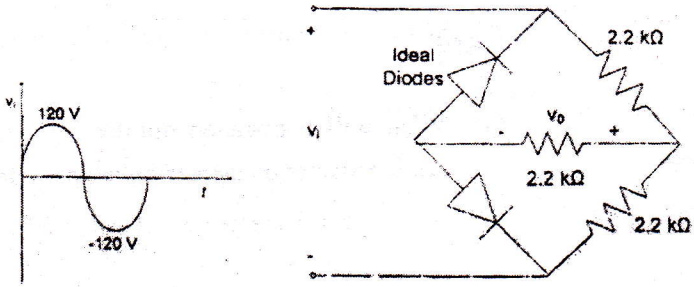
(i) What are don't care conditions in digital systems ?

(j) Write-down the three major advantages of digital multimeter over analog multimeter.

SECTION—B

2. Attempt any **three** parts of the following. All questions carry equal marks : **(10×3=30)**

(a) Draw and explain the full-wave bridge rectifier. Also derive the V_{dc} for it. Sketch v_0 for the network of Figure 1.



(b) Draw the circuit diagram of a BJT Emitter Bias and derive the expression for Quotient Point. Write its advantage over BJT fixed bias circuit. Also define bias stabilization and stability factors.

(c) Draw the structure of an n-channel JFET and explain its principle of operation. Also draw its drain and transfer characteristics with the help of suitable circuit. Describe how an FET can be used as a voltage controlled resistor.

(d) Explain the basic principle of signal display in a CRO. Also describe the method of measurement of frequency, amplitude and phase.

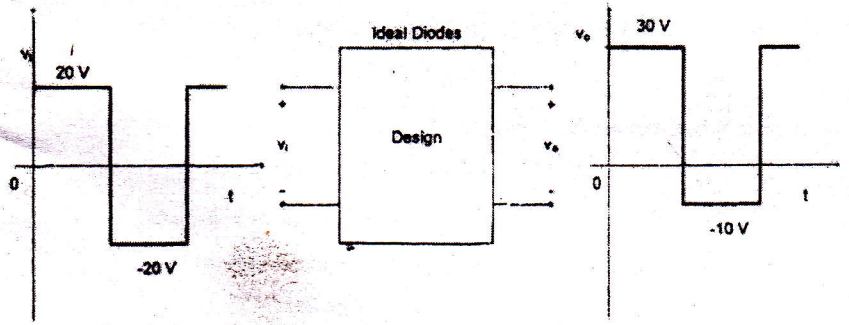
(e) What are universal gates, explain with neat sketch. Minimize and realize $f = \Sigma (1, 2, 5, 7, 9, 11, 12, 14, 15)$ using one type of universal gates only.

SECTION—C

Note :– All questions are compulsory. All questions carry equal marks.

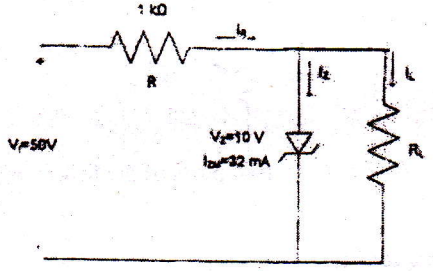
3. Attempt any two parts of the following. All questions carry equal marks : **(10×5=50)**

(a) Design a clamper to perform the function indicated in Figure 2.



(b) Explain the half wave voltage doubler and full wave voltage doubler with help of suitable diagrams.

(c) For the network of Figure 3, determine the range of R_L and I_L that will result in V_{RL} being maintained at 10 V. Also determine the maximum wattage rating of diode.



4. Attempt any **two** parts of the following. All questions carry equal marks :

(a) Explain the input and output characteristics of a BJT in the common emitter configuration. If the base current in transistor is 30 μA when the emitter current is 7.2 mA, what are the values of α and β ?

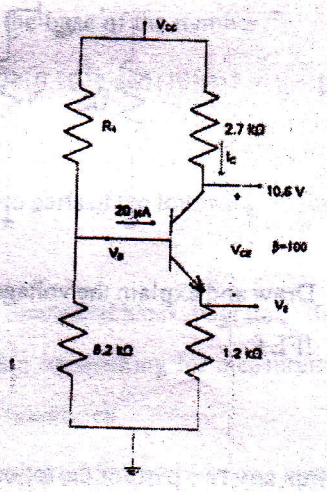
(b) Draw the hybrid equivalent circuit for common base configuration and write the expression for A_i, R_i, A_v and R_o.

(c) Determine the following for the voltage divider configuration shown in Figure 4 :

(i) I_C (ii) V_E

(iii) V_{CC} (iv) V_{CE}

(v) V_B (vi) R_1



5. Attempt any two parts of the following. All questions carry equal marks :

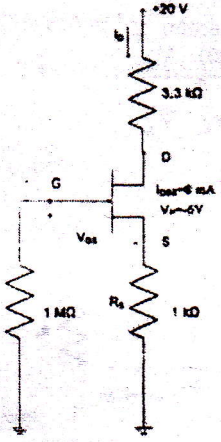
(a) What is the significant of the threshold voltage V_T in (i) depletion mode (ii) enhancement mode MOSFETs ?

(b) Determine the following for the network of Figure 5 :

(i) V_{GSQ} (ii) I_{DQ}

(iii) V_{DS} (iv) V_S

(v) V_G (vi) V_D



(c) Draw and explain the voltage divider bias configuration of JFET.

6. Attempt any two parts of the following. All questions carry equal marks :

(a) (i) Develop a circuit for $Y = (\bar{A} + B)CD$ Boolean expression using only NAND gates.

(ii) Develop a circuit for $Y = (A + B)C$ Boolean expression using only NAND gates.

(b) What do you mean by literal ?

Minimize the following using K-map technique :

$$f(A, B, C) = \Sigma m(1, 3, 6, 7) + \Sigma d(2, 4)$$

(c) Perform the following :

(i) Transform the following canonical expression into its other canonical form in decimal notation :

$f(A, B, C, D) = \pi M (0, 1, 4, 7, 9, 12, 15)$

(ii) Subtract by using $(r - 1)$'s complement method where r is the base of the number :

$(100110.101)_2$ and $(101011.01)_2$, $(6552)_{10}$ and $(9823)_{10}$

7. Attempt any two parts of the following. All questions carry equal marks.

(a) Draw the functional block diagram of the digital multimeter and explain its working for measurement of AC and DC electrical quantities.

(b) Define the horizontal and vertical sensitivity of a C.R.T.

(c) What is unity gain buffer ? Also draw and derive the expression for integrator using operational amplifier.