U - 3034 / 2927

Printed Pages : 7 TEC-201/101

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3034 Roll No.

B. Tech.

(SEM. II) EXAMINATION, 2007-08

ELECTRONIC ENGINEERING

Time : 3 Hours] *[Total Marks : 100*

Note : (1) Attempt **all** questions.

(2) All question carry **equal** marks.

(3) In case of numerical problems assume data whenever not provided.

(4) Be precse in your answer.

1 Attempt any **four** parts : **5×4**

(a) The mobility of free electrons and holes in pure germanium are 3800 and 1800 m^2 / Vs respectively. The corresponding values for pure silicon are 1300 and 500 m^2 / Vs respectively. Determine the values of intrinsic conductivity for both. Assume $n_i = 2.5 \times 10^{13}$ cm^{-3} for germanium and $n_i 1 = 2.5 \times 10^{10}$ cm^{-3} for silicon at room temperature.

(b) Describe the difference between majority and minority carriers.

(c) Define the static and dynamic resistance of the diode, how these resistances are measured.

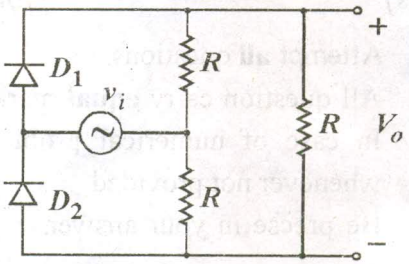
(d) Discuss the difference between diffusion and transition capacitances.

(e) Draw the reverse characteristics of a diode; define avalanche and Zenor breakdown regions.

(f) Define the reverse recovery time of a diode.

2 Attempt any **four** parts of the following : 5×4

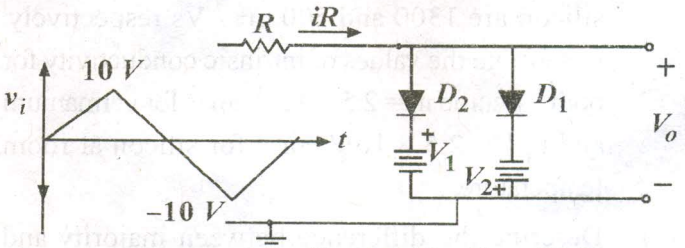
(a) Sketch Vo for the circuit shown in **fig. 1** D1 and D2 are silicon diodes.



$v_i = 100 \sin 314t$

Fig. 1

(b) For the circuit shown in **fig. 2** sketch iR and Vo. (D1 and D2 are Si diode.)



$V_1 = 5.3\ V \quad V_2 = 7.3\ V$

D_1 and D_2 are Si diodes

Fig. 2

(c) Determine V_L, I_L, I_Z and I_R for the circuit R_L is 470 ohms.

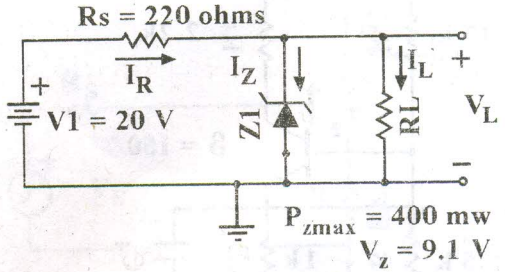


Fig. 3

(d) For the clamping circuit shown in **fig. 4** sketch for V0.

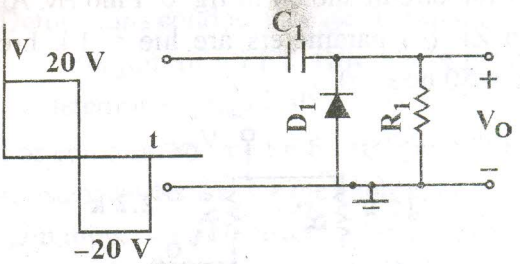


Fig. 4

(e) Draw the circuit diagram of a bridge rectifier. Discuss the operation and find dc and rms output voltage.

(f) With the help of the circuit diagram explain the working of a voltage doubler.

3 Attempt any **two** parts of the following : **10×2**

(a) For a voltage divider biasing circuit shown in fig. 5. Find I_C, V_{CE}, I_B, V_E and V_B.

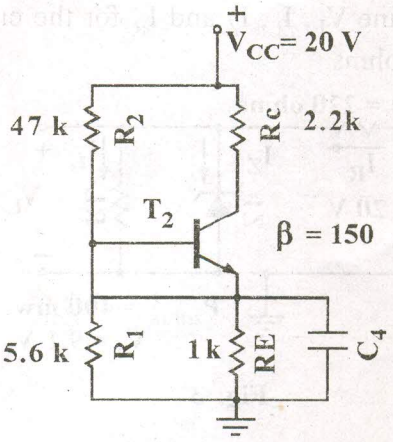


Fig. 5

(b) For the circuit shown in fig. 6. Find Av, Ai, Zo and Zi. (h) parameters are hie = 1 k hre = 0 hfe = 50 hoe = 0.

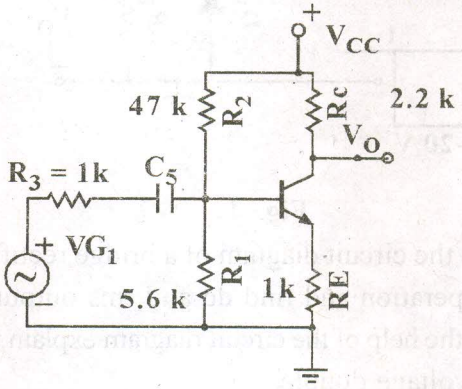


Fig. 6

(c) Derive the expression for input impedance and voltage gain for a CE and shown in **fig. 7** using simplified (approximate) equivalent circuit i.e. hre = hoe = 0.

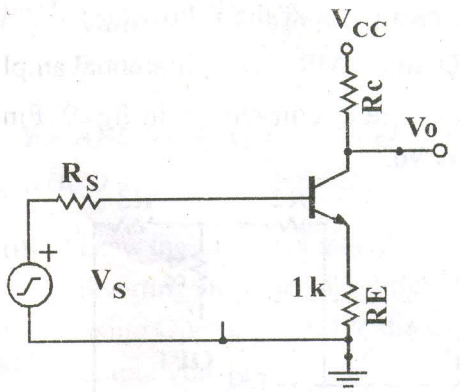


Fig. 7

4 Attempt any **two** parts of the following : **10×2**

(a) Define trans conductance (gm) output resistance (rp) and gain of a FET. How these parameters are determined graphically.

(b) For common source FET amplifier with source resistance is Rs. Derive the expression for voltage gain input impedance and output impedance.

(c) For a circuit shown in fig. 8. Calculate Vo, Zi and Zo. Input is Vi = 0.2 V (rms.)

I_{DSS} = 9 ma Vp = –4.5 V.

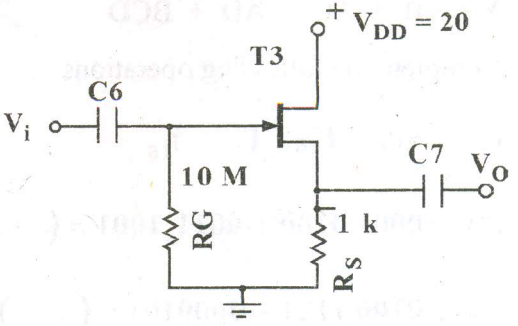


Fig. 8

5 Attempt any **two** parts of the following : **10×2**

(a) (i) Define CMRR of a differential amplifier.

(ii) For the circuit shown in fig. 9. Find out voltage, Vo.

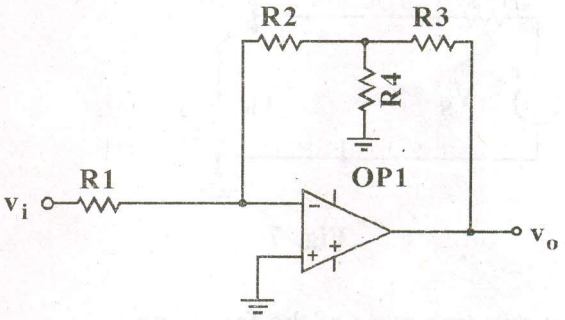


Fig. 9

(b) (i) Convert the following numbers :

(1) $2D6_{16} = (\quad)_2$

(2) $011010110_2 = (\quad)_{16}$

(ii) Convert the following function in to canonical forms :

$Y = AB + AC + AD + BCD$

(iii) Complete the following operations :

(1) $8_{16} + F_{16} = (\quad)_{16}$

(2) $0001\ 0100 + 0011\ 1001 = (\quad)_2$

$0100\ 1111 - 0000101 = (\quad)_2$

(iv) Minimize the following function using Boolean algebra.

$$Y = \bar{A}BCD + AB\bar{C}\bar{D} + AB\bar{C}D + ABCD + ABC\bar{D} + A\bar{B}\bar{C}D + A\bar{B}CD + A\bar{B}C\bar{D}$$

(c) (i) Draw the circuits of inverting amplifier, non-inverting amplifier and difference amplifier using Op-Amp. Derive the expression for output voltage.

(ii) Draw the circuit of integrator and differentiate using Op-Amp, derive the expression for output.
