Printed Pages : 8 EEC-201

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3302 Roll No. | | | | | | | | | | |

B. Tech.

(Second Semester) Theory Examination, 2010-11

ELECTRONICS ENGINEERING

Time : 3 Hours] *[Total Marks : 100*

Note : Attempt *all* questions.

1. Attempt each of the following parts : 2×10=20

(a) If V_m is peak voltage across secondary of a transformer in a bridge full wave rectifier, then peak inverse voltage is given by :

(i) V_m

(ii) $V_m/2$

(iii) $2V_m$

(iv) None of them.

(b) The Avalanche breakdown in semiconductor diode occurs when :

(i) Forward current exceeds a certain value

(ii) Reverse bias exceeds a certain value

(iii) Forward bias exceeds a certain value

(iv) The potential barrier is reached to zero.

(c) A transistor is operating in active region, under this condition :

(i) both the junctions are forward bias

(ii) both the junctions are reverse bias

(iii) Emitter base junction is reverse bias collector base junction is forward bias

(iv) Emitter base junction is forward bias collector base junction is reverse bias.

(d) An amplifier circuit of voltage gain 100, 2V output voltage the input voltage applied is ..... .

(e) In enhancement *n*-channel MOSFET an induces *n* type channel can be produced between the source and drain if V_{gs} is negative . (True/False)

(f) Inverting amplifier gain is independent of source resistance. (True/False)

(g) The output voltage in OPAMP differentiator with input voltage V_i the output voltage is given by ..... when $R = 1K$ and $C = 1pf$.

(h) $(CA95.12)_{16} - (9FE.A)_{16} =$ .....

(i) $A'B'C' + A'B'C + A'BC' + ABC' =$ .....

(j) The sweep voltage is applied on the ..... axis of CRO.

2. Attempt any *four* parts : 5×4=20

(a) Draw the circuit diagram of full wave bridge rectifier and explain the operation and also draw the input and output waveform.

(b) Determine the currents I_1, I_2 and I_{D_2} for the network shown below (Fig. 1) :

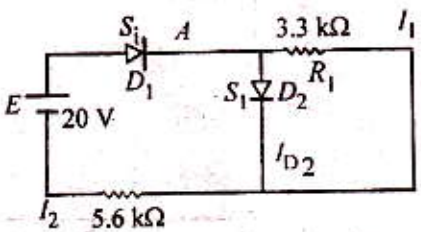


Fig. 1

(c) For the Zener diode network of the Fig. 2, determine V_L, V_R, I_Z and P_Z.

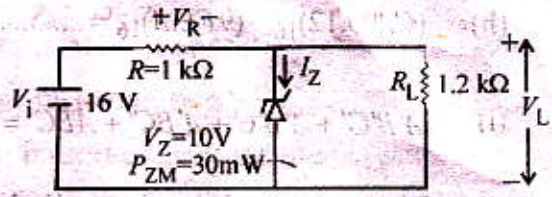
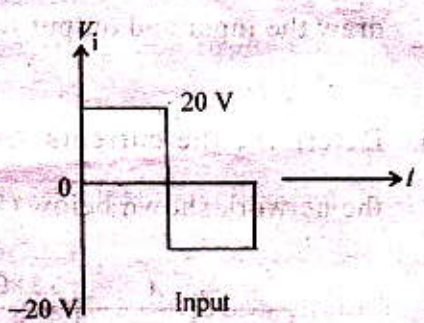


Fig. 2

(d) Sketch V_o for the network of Fig. 3 for the input shown :



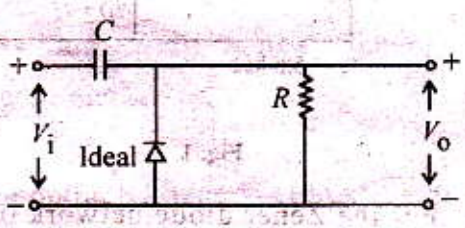


Fig. 3

(e) Draw the voltage Tripler circuit and explain the operation.

(f) Determine I, V_1, V_2 and V_0 for the series of dc configuration in Fig. 4.

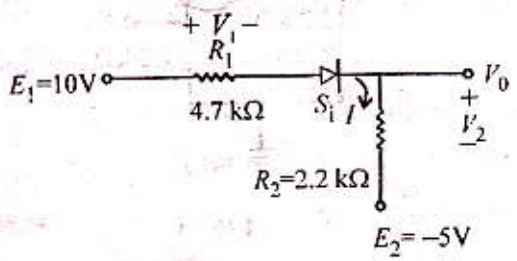


Fig. 4

3. Attempt any *two* parts : 10×2=20

(a) Draw the input and output characteristics ($v-i$) of a CE npn transistor configuration with proper levels and discuss how you will determine h_{ie} and h_{fe} hybrid parameters from these characteristics.

(b) For the voltage-divider bias configuration of Fig. 5 determine (i) I_C (ii) V_E (iii) V_{CC} (iv) V_{CE} (v) V_B (vi) R_1.

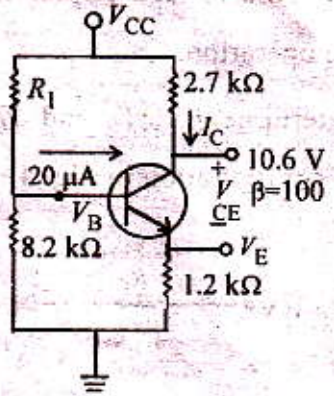


Fig. 5

(c) For the emitter-stabilized bias circuit of Fig. 6, determine (i) I_{B_2} (ii) I_{C_2} (iii) V_{CE_2} (iv) V_C (v) V_B (vi) V_E.

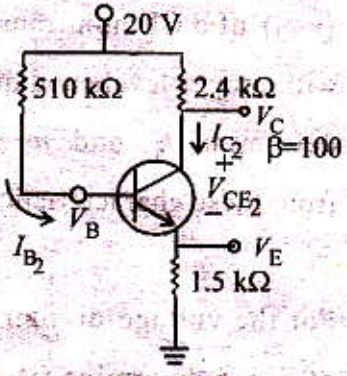


Fig. 6

4. Attempt any *two* parts : 10×2=20

(a) What is the significant difference between the construction of an enhancement-type MOSFET and depletion-type MOSFET ? Sketch the basic construction of a *p*-channel depletion-type MOSFET.

(b) Draw a neat schematic diagram of a cathode ray tube with proper labels. How is the intensity of the spot/trace controlled in a cathode ray oscilloscope ?

(c) (i) Sketch a three-input inverting summing circuit and derive an expression for the output voltage.

(ii) Design a non-inverting amplifier circuit that is capable of providing a voltage gain of 15. Assume ideal op-amp and resistances used should not exceed 30 kΩ .

5. Attempt any *four* parts : 5×4=20

(a) Simplify the following function by using the Boolean algebra :

(i) $A\overline{B}\,\overline{C}D + \overline{A}\,\overline{B}D + BC\,\overline{D} + \overline{A}B + B\overline{C}$

(ii) $(AB + \overline{A}C + BC)(A + \overline{B} + A\overline{B})$.

(b) Perform the following binary arithmetic operations :

(i) $(1101.1101)_2 - (1001.10)_2$

(ii) $(AB9.54)_{16} + (39C.CD)_{16}$.

(c) Simplify the function using K-map :

$f(A, B, C, D) =$

$\Sigma m(3, 4, 5, 7, 9, 13, 14, 15) + \Sigma d(0, 1, 8, 10)$

Implement the output using gates.

(d) (i) Convert the given expression into canonical SOP form :

$$f = A + AB + ABC .$$

(ii) Convert the given expression into canonical POS form :

$$f = (A + B)(B + C) + (C + A) .$$

(e) What is the universal gate ? Name the universal gate ? Give the proof of universal gate at least for one type of gate.

(f) Draw the block diagram of digital multimeter. Explain the operation of each block.