(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3072 Roll No.

B.Tech

(SEM III) ODD SEMESTER THEORY EXAMINATION 2009-10

SWITCHING THEORY

Time : 3 Hours] *[Total Marks : 100*

Note : *(i) All questions carry equal marks.*
(ii) All questions are compulsory.

1 Attempt any four of the following : 5×4=20

(a) What are Gray codes ? Give its advantages. Convert 10111011 in binary into its equivalent gray code.

(b) What is the range of 16 bit unsigned numbers, 16 bit signed magnitude numbers 16-bit signed two's complement numbers and 16-bit signed one's complement numbers. How many representations are possible for '0' decimal is one's complement and two's complement representation. Prove your answer.

(c) Represent decimal number 8620 in
(i) Binary
(ii) BCD
(iii) Excess-3 and
(iv) 2421 codes.

(d) What is the largest number that can be obtained with 16 bits ? What is its decimal equivalent ?

(e) Find the sum of the following pairs of decimal numbers assuming 8-bit 1's complement representation of numbers

(i) $+61+(-23)$

(ii) $-56+(-55)$.

(f) Convert the the binary number 1001110 into Hamming code.

2 Attempt any **four** of the following : 5×4=20

(a) Simplify the following boolean function using K-map

$$f(w, x, y, z) = \sum(1, 3, 7, 11, 15)$$

and don't care condition is

$$d(w, x, y, z) = \sum(0, 2, 5)$$

Express the reduced form in SOP and POS forms.

(b) Simplify the following boolean function by Tabulation method

$$f = \sum(0, 1, 2, 8, 10, 11, 14, 15)$$

(c) Discuss the disadvantage of 4-bit binary parallel adder and design the logic and circuit of 4-bit full adder with look-ahead carry.

(d) (i) Implement full subtractor using Demultiplexer.

(ii) Design 5-to-32 decoder using one 2-to-4 and four 3-to-8 decoders.

(e) Design the circuit for BCD to excess-3 code converter.

(f) Give the comparison between PROM, PLA and PAL. Implement following boolean function using PLA

[$X(A, B, C) = \sum m(0, 1, 3, 5)$,

$Y(A, B, C) = \sum(0, 1, 2, 4, 6)$,

$Z(A, B, C) = \sum m(0, 2, 6, 7)$ and

$W(A, B, C) = \sum m(3, 6)$].

3 Attempt any **two** of the following : 10×2=20

(a) Design a synchronous BCD counter with JK flip flops.

(b) (i) Define critical and non critical race.

(ii) With the help of two shift registers design a 4-bit serial adder.

(c) (i) Explain ASM technique for designing sequential ckt.

(ii) Draw an ASM chart for a 2-bit binary counter having one enable line E such that

$E = 1$ (counting enabled)

$E = 0$ (counting disabled)

4 Attempt any **two** of the following : **10×2=20**

(a) Design an asynchronous sequential circuit that has two inputs X_2 and X_1 and one output Z. When $X_1 = 0$ the output Z is 0. The first change in X_2 that occurs while X_1 is 1 will cause output Z to be 1. The output Z will remain 1 until X_1 returns to 0.

(b) (i) Draw and explain the basic CMOS inverter circuit.

(ii) Give the characteristics of ECL family.

(c) What are Hazards ? Give hazard free realisation for the following boolean function

$f(A, B, C, D) = \sum m(2, 3, 5, 7, 10, 14)$

5 Attempt any **two** of following : **10×2=20**

(a) Explain the working of dynamic RAM cell. Explain the read cycle timing and write cycle timing of RAM with the help of neat timing diagram.

(b) Obtain a **16×8** memory using **16×4** memory ICs and draw the concerned IC circuit.

(c) Draw the circuit of MOSFET RAM cell and explain its operation.
