

(Following Paper ID and Roll No. to be filled in your Answer Book)

**PAPER ID : 3071**

Roll No.

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### B.Tech.

(SEM. III) ODD SEMESTER THEORY EXAMINATION

2010-11

### PULSE AND DIGITAL ELECTRONICS

Time : 3 Hours

Total Marks : 100

Note :- Attempt all questions. All questions carry equal marks.

1. Attempt any two parts of the following : (10×2=20)

(a) Draw the circuit diagram of NMOS NOR gate and explain its operation. Why power dissipation in an NMOS NAND gate is lower than that of NMOS NOR gate ? Explain.

(b) Simplify the given function using tabular method  
 $F(A, B, C, D, E, F, G) = \Sigma(20, 28, 38, 39, 52, 60, 102, 103, 127)$ .  
 Also implement the simplified function using basic gates.

(c) Simplify the given function using Karnaugh Map :

$$F(A, B, C, D) = \Sigma(0, 2, 3, 6, 7)$$

$$d(5, 8, 10, 11, 15).$$

Also implement the simplified function using univesal gates only.

2. Attempt any four parts of the following : (5×4=20)

(a) Subtract 68 from 61 using BCD. Show all the steps.

(b) Design Full Subtractor. Also show truth table and circuit diagram.

(c) Design a 3-bit magnitude comparator.

(d) Design a full adder using 8 : 1 multiplexer.

(e) Implement the following function using PLA :

$$F_1(A, B, C) = \Sigma (0, 1, 6, 7)$$

$$F_2(A, B, C) = \Sigma (1, 2, 4, 6).$$

(f) A combinational circuit is defined by the following Boolean functions. Design circuit with a decoder and external gates :

$$Y_1 = \bar{A} \bar{B} \bar{C} + AC$$

$$Y_2 = A \bar{B} C + \bar{A} C.$$

3. Attempt any four parts of the following : (5×4=20)

(a) What is the difference between a latch and a flip-flop ?  
How basic latch operation is performed by NOT gates ?

(b) Convert D - flip-flop to T flip-flop.

(c) Design universal shift register.

(d) Design a Mod-5 synchronous counter.

(e) Design a four-stage Johnson Counter.

(f) Draw waveforms to illustrate how a serial binary number 1011 is loaded into a shift register.

4. Attempt any four parts of the following : (5×4=20)

- With the help of figure explain the operation of a bipolar SRAM cell and MOS SRAM cell.
- Explain basic semiconductor memory organization with the help of figure.
- Explain the working of dual slope ADC.
- Explain the operation of basic sample and hold circuit. Also state the advantages and applications of sample and hold circuits.
- What is attenuator ? Explain the under and over compensation in attenuators.
- Derive and draw the response of low pass RC circuit to step and sinusoidal waveforms.

5. Attempt any four parts of the following : (5×4=20)

- With reference to a PLL, define :
  - Caputure range
  - Lock range
  - Pull in time.
- For a noninverting regenerative comparator shown in Fig. 1, calculate tripping voltages. Assume  $V_{sat} = \pm 12\text{ V}$

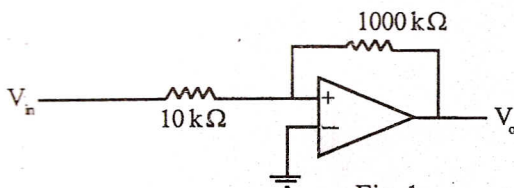


Fig. 1

- (c) Design a monostable for a pulse width of 10 ms by using IC 555.
- (d) Explain the working of IC 555 as an astable multivibrator with neat diagram.
- (e) Design an adjustable voltage regulator using IC 7805 to give variable output voltage from +5 V to +8 V with  $I_L = 1$  A.
- (f) Draw the diagram of series and shunt regulators and explain the working.