(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 1249 Roll No. | | | | | | | | | | |

B.Tech.

(SEM. III) ODD SEMESTER THEORY EXAMINATION 2013-14

DIGITAL DESIGN

SECTION–A

1. Attempt **all** parts : **(10×2=20)**
   (a) Convert $(FAFA.B)_{16} = (?)_{10}$.
   (b) Simplify the following Boolean Expressions (x + y) (x + y') to a minimum no. of literals.
   (c) How many address lines and input-output data lines are needed in 256 K × 64 ?
   (d) How many Flip-Flops are required to design MOD-6 counter ?
   (e) Define the excutation table of S-R flip-flop.
   (f) Explain the difference between a Johnson counter and a ring counter.
   (g) Convert binary no. 101011 into gray code.
   (h) Design Ex OR gate using NAND gate only.
   (i) Find the complement of $(\bar{x} + \bar{y} + z)(\bar{x} + y)(x + \bar{z})$.
   (j) Explain Volatile and Non Volatile memory.

SECTION–B

2. Attempt any **three** parts : **(3×10=30)**
   (a) (i) Simplify the function in sum-of-minterms form :
   F (A, B, C, D) = Σ (4, 5, 6, 7, 12, 13, 14)
   d (A, B, C, D) = Σ (1, 9, 11, 15) using Tabular Method
   (ii) Implement the following Boolean function f, using the two-level forms of logic :
   (a) NAND-AND
   (b) AND-NOR

(c) OR-NAND and

(d) NOR-OR.

$F(A, B, C, D) = \Sigma (0, 4, 8, 9, 10, 11, 12, 14)$

(b) (i) Define a combinational circuit with three inputs x, y, and z and three outputs A, B and C. When the binary input is 0, 1, 2 or 3, the binary output is two greater than the input. When the binary input is 4, 5, 6 or 7, the binary output is two less than the input.

(ii) Implement the following Boolean function with a 4×1 MUX and external gates.

$F(A, B, C, D) = \Sigma (1, 3, 4, 11, 12, 13, 14, 15)$

(c) (i) A sequential circuit has two JK flip flops A and B and one input x. The circuit is described by the following flip flop input equations :

$J_A = x \qquad K_A = B'$

$J_B = x \qquad K_B = A$

(a) Derive the state equations A (t + 1) and B(t + 1) by substituting the input equations for the J and K variables.

(b) Draw the state diagram of the circuit.

(ii) Show that a BCD ripple counter can be constructed from a four-bit binary ripple counter with asynchronous clear and a NAND gate that detects the occurrence of count 1010.

(d) (i) Draw the logic diagram of the product-of-sums expression :

$Y = (x_1 + x_2')(x_2 + x_3)$.

Show that there is a static-O hazard when x_1 and x_3 are equal to 0 and x_2 goes from 0 to 1. Find a way to remove the hazard by adding one more OR gate.

(ii) Obtain a primitive flow table for a circuit with two inputs x_1 and x_2 and two outputs z_1 and z_2, that satisfy the following four conditions :

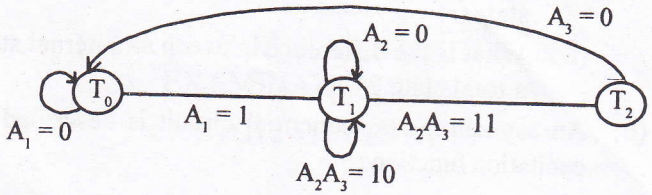
(a) When $x_1x_2 = 00$, the O/P is $z_1z_2 = 00$

(b) When $x_1 = 1$ and x_2 changes from 0 to 1, the O/P is $z_1z_2 = 01$.

(c) When $x_2 = 1$ and x_1 changes from 0 to 1, the O/P is $z_1 z_2 = 10$.

(d) Otherwise, the O/P does not change.

(e) (i) Design the controller whose state diagram is shown in fig. Use one-flip-flop per state method.



(ii) Obtain the 15-bit Hamming code word for the 11-bit data word 11001001010.

SECTION–C

3. Attempt any **one** part : **(5×10=50)**

(a) Find all the prime implicants for the following Boolean function, and determine which are essential :

$F(A, B, C, D) = \Sigma (0, 2, 3, 5, 7, 8, 10, 11, 14, 15)$

(b) Simplify the following Boolean function, using five variable maps :

F (A, B, C, D, E) = A' B' C E' + B' C' D' E' + A' B' D' + B' C D' + A' C D + A' B D.

4. Attempt any **one** part :

(a) Implement a full subtractor with a decoder and NAND gates. The adder inputs are A, B and C. The adder produces outputs S and C.

(b) What is the difference between flow chart and ASM chart ? Also draw an ASM chart state table for a two bit up-down counter having mode control input. M = 1 (up counting) and M = 0 (down counting). The circuit should generate an output 1, whenever count become minimum or maximum.

5. Attempt any **one** part :

(a) Design MOD-12 Synchronous Counter.

(b) Explain the four bit Universal Shift Register.

6. Attempt any **one** part :

(a) (i) Explain the difference between asynchronous and synchronous sequential circuits.

(ii) Define fundamental-mode operation.

(iii) Explain the difference between stable and unstable states.

(iv) What is the difference between an internal state and a total state ?

(b) An asynchronous sequential circuit is described by the excitation function :

$Y = x_1 x_2' + (x_1 + x_2')y$ and O/P $z = y$.

(i) Draw the logic diagram of the circuit.

(ii) Derive the transition table and output map.

(iii) Obtain a two-state flow table.

(iv) Describe the behavior of the circuit.

7. Attempt any **one** part :

(a) Derive the PLA programming table for the combinational circuit that squares a three-bit number.

(b) Design the ROM circuit for the BCD to excess-3 code converter.