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NEC-309

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 110310

Roll No.

B.Tech.

(SEM. III) (ODD SEM.) THEORY EXAMINATION, 2014-15

DIGITAL LOGIC DESIGN

Time : 3 Hours] [Total Marks : 100

Note : (1) Attempt all questions

(2) Allocated marks are indicated against each question.

(3) Assume any missing data suitably.

1 Attempt any **Four** parts : (4×5=20)

(a) Explain weighted and unweighted code with example.

(b) Convert the following numbers as indicated :

(i) $(BC64)_{16} = (\ )_{10} = (\ )_{2}$

(ii) $(111011)_{2} = (\ )_{5}$

(c) Draw a NAND logic diagram that implements the complement of the following function

$F(A,B,C,D) = \sum (0,1,2,3,4,8,9,10,11,12)$.

(d) Draw suitable diagram of full adder.

(e) Design and explain the logic and circuit of 4 bit magnitude comparator.

(f) What is race around condition ? Explain in brief.

2 Attempt any **four** parts : **(4×5=20)**

(a) Differentiate between EPROM and EEPROM.

(b) A certain memory has a capacity of 8K × 16. How many bits are there in each word ? How many words are being stored ?

(c) Differentiate between truth table, excitation table, state table. Design D flipflop using SR flipflop.

(d) (i) The Hamming code 101101101 is received with even parity. Correct errors (if any).

(ii) Simplify $\overline{A}'B\overline{C}\overline{D}' + BC\overline{D}' + B\overline{C}'\overline{D}' + B\overline{C}'D$.

(e) Design 16:1 multiplexer using 4:1 multiplexer.

(f) Explain priority encoder.

3 Attempt any **Two** parts : **(10×2=20)**

(a) Minimize the given Boolean function using K map and implement the simplified function using NAND gates only.

$F(A,B,C,D) = \sum m\ (0,1,2,9,11,15) + d(8,10,14)$.

(b) Minimize the following functions by tabular method

$F(w,x,y,z) = \sum m\ (0,2,3,6,7,8,10,12,13)$.

(c) Design a 4 bit combinational circuit which converts BCD to Excess-3 code.

4 Attempt any **Two** parts : **(10×2=20)**

(a) Design a 3 bit combinational circuit which produce logic 1 output when more than one input variables are at logic 1.

(b) Implement the following functions using 3 input, 4 product term and 2 output using PLA

$F1 = A\overline{B}' + AC + \overline{A}'B\overline{C}'$

$F2 = (AC + BC)^*$

(c) A sequential circuit with two D flip-flops A and B and an input X and output Y. The circuit is described by the following next state and output equations.

$A(t+1) = AX + BX$

$B(t+1) = \overline{A}'X$

$Y = (A+B)\overline{X}'$

(i) Derive the state table.
(ii) Draw the logic diagram of the circuit.
(iii) Derive the state diagram.

5 Attempt any **Two** parts : **(10×2=20)**

(a) What do you understand by fundamental mode of operation ? Explain different types of Hazards in Asynchronous sequential circuit by giving suitable example.

(b) Draw and explain the working of universal shift register.

(c) An asynchronous sequential circuit has two internal states and output. The excitation and Output functions describing the circuit are as follows.

$Y = x_1x_2 + (x_1 + x_2)Y$ and $Z = Y$.

(i) Draw the logic diagram.
(ii) Derive the transition table and output map.
(iii) Obtain the flow table of circuit.
