(Following Paper ID and Roll No. to be filled in your Answer Books)

Paper ID : 2289954 Roll No. | | | | | | | | | |

B.TECH.

Regular Theory Examination (Odd Sem - III),2016-17

DIGITAL LOGIC DESIGN

Time : 3 Hours *Max. Marks : 100*

Note: Attempt All sections. If require any missing data: then choose suitably.

Section - A

1. Attempt all questions in brief. (10×2=20)

a) Perform 2's complement subtraction of 010110-100101.

b) What is the feature of gray code?

c) Write the logic equation and draw the internal logic diagram for a 4 to 1 mux.

d) What is a priority encoder?

e) List the major differences between PLA and PAL.

f) Define a Bus. What are the different types of buses?

g) Give the comparison between combinational circuits and sequential circuits.

h) What are the different types of flip-flop?

i) Give the comparison between synchronous & asynchronous sequential circuits.

j) When does race condition occur?

Section - B

2. Attempt any three of the following: (3×10=30)

a) Reduce the Boolean function using k-map technique and implement using gates

$f(w,x,y,z) = \sum m(0,1,4,8,9,10)$ which has the don't cares condition $d(w,x,y,z) = \sum m(2,11)$

b) Implement the following multiple output combinational logic circuit using a 3 to 8 decoder.

i) $f_1 = \sum m(1,2,3,5,7)$

ii) $f_2 = \sum m(0,3,6)$

iii) $f_3 = \sum m(0,2,4,6)$

c) What is Ram? Explain the different types of RAM in detail.

d) Realize

i) A JK flip flop using SR flip flop.

ii) A SR flip flop using NAND gates and explain its operation.

Section - C

3 Attempt any one part of the following (1×10=10)

a) Detect and correct error (if any) in the following received even parity Hamming code word 00111101010.

b) Minimize the given Boolean function using Quine Mc Clusky method

$f(A,B,C,D) = \sum m(0,1,2,4,5,8,9,11,15)$ and implement the simplified function using NOR gates only.

4. Attempt any one part of the following (1×10=10)

a) i) Obtain the simplified Boolean expression for the output F and G in terms of the input variables in the circuit of fig. 1

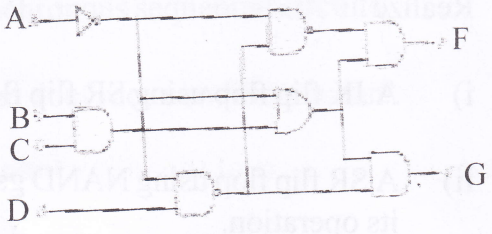

Fig. 1

ii) Implement the full adder and full subtractor using decoder.

b) i) Design a combinational circuit that compares the magnitude of two 3 bit numbers and its output indicates whether A>B, A = B, A<B.

ii) Construct a BCD to excess 3 code converter with a 4 bit adder. What must be done to change the circuit to an excess 3 to BCD code converter?

5. Attempt any one part of the following (1×10=10)

a) Design a combinational circuit using a ROM. The circuit accepts a three-bit number and outputs a binary number equal to the square of the input number.

b) Draw a PLA circuit to implement the functions

$f_1 = A'B + AC' + A'BC'$, $f_2 = (AC + AB + BC)'$,

$f_3 = BC + AC + A'BC'$

6. Attempt any one part of the following (1×10=10)

a) A sequential circuit has three flip flop A,B and C; one input x in and one output y out. The state diagram is shown in fig2. The circuit is to be designed by treating the unused states as don't-care conditions. Use T flip flop in the design.

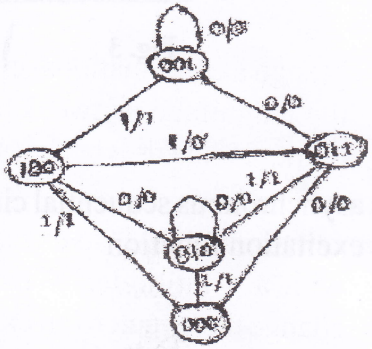

Fig. 2

b) Design a 4 bit binary synchronous counter with D flips flop.

7. Attempt any one part of the following (1×10=10)

a) Derive the transition table for the asynchronous sequential circuit shown in fig.3 determine the sequence of internal states Y_1Y_2 for the following sequence of input X_1X_2: 00,10;,11,01,11,10,00.

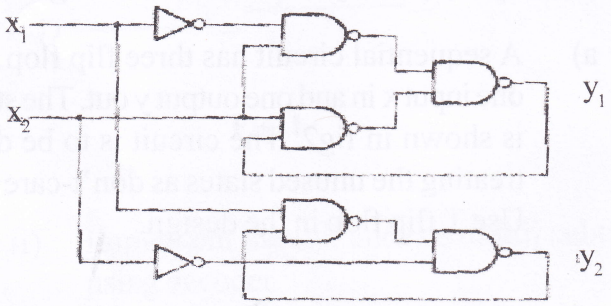

Fig. 3

b) An asynchronous sequential circuit is described by the excitation function

$Y = x_1 x_2' + (x_1 + x_2')y$ and $z = y$

i) Draw the logic diagram of the circuit

ii) Drive the transition table and output map.
