(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 1067 Roll No. | | | | | | | | | | |

B. Tech.

(SEM. IV) THEORY EXAMINATION 2010-11

COMPUTER ORGANIZATION

Time : 3 Hours *Total Marks : 100*

Note :– Attempt ***all*** questions.

1. Attempt any **FOUR** parts of the following :— **5×4=20**

(a) Show the hardware that implements the following statements. Include the logic gates for the control function and a block diagram for the binary counter with a count enable input :

$$xyT_0 + T_1 + y'T_2 : AR \leftarrow AR + 1.$$

(b) Draw logic diagram of Arithmetic curcuit that performs Addition, Subtraction, Increment and Decrement operations.

(c) Show the multiplication process using Booth's algorithm when the following binary numbers are multiplied :

$$(-12) * (-18).$$

(d) Write a procedure to add two IEEE single-precision floating point numbers. Each number is represented by a 32-element Boolean array.

(e) Discuss the Bus Arbitration.

(f) Show the block diagram of the hardware that implements the following register transfer statement :

$$yT2 : R2 \leftarrow R1, R1 \leftarrow R2.$$

2. Attempt any **FOUR** parts of the following :— 5×4=20

(a) Show the control step for an unconditional Branch instruction for a processor that has single bus structure.

(b) Write the sequence of control steps required for the single bus structure for the following instruction :

Add ((R2)), R1.

(c) What are the relative merits of horizontal and vertical microinstruction format ?

(d) What are the advantages and disadvantages of hardwired and microprogrammed control ?

(e) Formulate a mapping procedure that provides eight consecutive microinstruction for each routine. The operation code has six bits and the control memory has 2048 words.

(f) An encoded microinstruction format is to be used. Show how a 9-bit microoperation field can be divided into subfields to specify 46 different actions.

3. Attempt any **TWO** parts of the following :— 10×2=20

(a) Write a program to evaluate the arithmetic statement :

$$X = (A + B * C) / (D - E/F).$$

(i) Using a general register computer with three address instructions.

(ii) Using general register computer with two address instructions.

(iii) Using an accumulator type computer with one address instructions.

(iv) Using a stack organized computer with zero-address operation instructions.

(b) Design a variable-length op code to allow all of the following to be encoded in a 36-bit instruction :

(i) Instruction with two 15-bit addresses and one 3-bit register number.

(ii) Instruction with one 15-bit address and one 3-bit register number.

(iii) Instruction with no addresses or registers.

(c) (i) How many times does the control unit refer to memory when it fetches and executes an indirect addressing mode instruction if the instruction is (I) a computational type requiring an operand from memory (II) a branch type ?

(ii) Let the address stored in the program counter be designated by the symbol XI. The instruction stored in X1 has an address part X2. The operand needed to execute the instruction is stored in the memory word with address X3. An index register contains the value X4. What is the relationship between these various quantities if the addressing mode of the instruction is (a) direct; (b) indirect; (c) PC relative; (d) indexed ?

4. Attempt any TWO parts of the following :— **10×2=20**

(a) With the help of block diagram, discuss working of direct memory access (DMA). Also explain main features of an IOP. Give a brief comparison of DMA and IOP.

(b) Design a parallel priority interrupt hardware for a system with eight interrupt sources.

(c) Compute the transfer rate in character per second for serial transmission of characters having 7 information

bits, a parity bit, 2 stop bits at a bit rate of 600 per second. Assume no idle time between characters. Compare the data transfer rate with synchronous transmission having the same bit rate and two sync characters followed by 100 seven bit information characters.

5. Attempt any **TWO** parts of the following :— **10×2=20**

(a) A set associative mapping cache has a set size of 4. The cache capacity is 2 K words and that of main storage is 128 K × 32. Derive all pertinent information required to design the Cache memory and note the data path for the set associative organization. Determine the average memory access time for a cache hit of 0·85, cache access time of 100 nsec and main storage access time of 500 nsec.

(b) A virtual memory system has 16 K word logical address space, 8 K word physical address space with a page size of 2 K words. The page address trace of a program has been found to be :

7 5 3 2 1 0 4 1 6 7 4 2 0 1 3 5

Note the four pages resident in the memory after each page reference change for each of the following replacement policies :

(i) FIFO

(ii) LRU

(iii) Anticipatory swapping.

(c) Write short notes on the following :—

(i) Virtual memory.

(ii) 2D memory organization.