Printed Pages : 3 EEC401

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0321 Roll No. | | | | | | | | | | |

B.Tech.

(SEMESTER-IV) THEORY EXAMINATION, 2011-12

ELECTRONIC CIRCUITS

Time : 3 Hours] *[Total Marks : 100*

Note : Attempt questions from **all** sections. Assume missing data if any.

Section – A

1. Answer **all** parts. $10 \times 2 = 20$

(a) What is the minimum number of terminals required by a single Op-Amp ? What is the minimum number of terminals required on an integrated-circuit package containing four Op-Amps ?

(b) Design a simple current divider that will reduce the current provided to a 1 KΩ load to 20% of that available from the source.

(c) Design an inverting closed loop amplifier having a gain of –10 and an input resistance of 100 KΩ. Calculate values of R_1 and R_2.

(d) Define full-power band-width in an Op-Amp.

(e) For NMOS transistor, write the drain current expression in Triode region and Saturation region.

(f) Draw a large-signal equivalent circuit model of the n-channel MOSFET in saturation, incorporating the output resistance.

(g) Calculate β for two transistors for which $\alpha = 0.99$ and 0.98.

(h) A BJT having $\beta = 100$ is biased at a dc collector current of 1 mA. Find the value of g_m and r_e.

(i) Define the input common – mode range of a Differential Amplifier.

(j) Define Transconductance and Trans-resistance Amplifiers.

Section – B

2. Attempt any **three** parts : $3 \times 10 = 30$

(a) (i) Consider the basic differential amplifier circuit with $R_1 = R_3 = 2\ k\Omega$ and $R_2 = R_4 = 200\ k\Omega$. Find the value of A_d, R_{id}, and R_0.

(ii) An Op-Amp having a slew-rate of 20 V/μs is to be used in the unity-gain follower configuration, with input pulse that rises from 0 to 3V. What is the shortest pulse that can be used while ensuring full-amplitude output ?

(b) A transistor amplifier is fed with a signal source having an open-circuit voltage v_{sig} of 10 mV and internal resistance R_{sig} of 100 kΩ. The voltage v_i at the amplifier input and output voltage v_0 are measured both without and with load resistance $R_L = 10\ k\Omega$ connected to the amplifier output. The measured results are as follows :

	v_i (mV)	v_0 (mV)
Without R_L	9	90
With R_L connected	8	70

Find all the amplifier parameters.

(c) Draw the circuit diagram of single stage CE amplifier, implement hybrid-π model and T-model for it and calculate expressions for i_e, g_m and i_b.

(d) Draw the NMOS differential amplifier with a common-mode input signal and calculate the Common Mode Gain and CMRR. Also explain the effect of R_D mismatch on CMRR.

(e) Design a series – series feedback amplifier and calculate expressions for A_f, R_{of} and R_{if}.

Section – C

Attempt **all** parts. $5 \times 10 = 50$

3. Attempt any **two** parts.

(a) A MOSFET is to operate at $I_D = 0.1$ mA and is to have $g_m = 1$ mA/V. If $k_n = 50\ \mu A/V^2$, find the required W/L ratio and the overdrive voltage.

(b) Draw the high-frequency equivalent circuit model for the MOSFET and list all MOSFET internal capacitances.

(c) For the CS amplifier, determine its low frequency transfer function.

4. Attempt any **two** parts.

(a) Draw the circuit diagram of biasing the MOSFET using a constant-current source and calculate the expression for I in terms of I_{REF}.

(b) Discuss the various internal capacitances in detail for BJT.

(c) Draw the circuit diagram of CB amplifier and calculate expression for short-circuit current gain with T-model.

5. Attempt any **two** parts.

(a) Consider a CE circuit using a BJT having $I_S = 10^{-15}$A, a collector resistance $R_C = 6.8\ k\Omega$, and a power supply $V_{CC} = 10$ V.

(i) Determine the value of the bias voltage V_{BE} required to operate the transistor at $V_{CE} = 3.2$ V. What is the corresponding value of I_C ?

(ii) Find the voltage gain A_V at this bias point.

(b) Explain how to operate the BJT as a switch.

(c) Calculate the R_{in} or R_{out} for the CC amplifier.

6. Attempt any **two** parts.

(a) Draw the circuit diagram of BJT differential pair and explain its large-signal operation.

(b) Calculate the transconductance G_m for the active-loaded MOS differential pair.

(c) For the active-loaded BJT differential amplifier let I = 0.8 mA, $V_A = 100$ mV and $\beta = 100$ find G_m & R_o.

7. Attempt any **two** parts.

(a) Explain how Negative feedback affects Gain, Band-width & Noise.

(b) Draw the circuit diagram of a Wien-bridge oscillator and derive an expression for the frequency of oscillations.

(c) For the Hartley Oscillator, derive an expression for the frequency of oscillation.
