(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 2117 Roll No. | | | | | | | | | | |

B.Tech.

(SEM. V) ODD SEMESTER THEORY EXAMINATION 2010-11

INTEGRATED CIRCUITS

Time : 3 Hours *Total Marks : 100*

Note : Attempt **all** questions.

1. Answer any **four** of the following : **(5×4=20)**
   (a) Explain the circuit of Wilson MOS current mirror. Also, discuss how it can be improved.
   (b) What do you understand by base current compensated current mirror ?
   (c) Discuss the DC analysis of Second Stage of 741 Op-Amp.
   (d) How the short circuit protection is achieved in the output stage of 741 Op-Amp ? Also, find the output resistance of 741 Op-Amp.
   (e) Figure 1 shows two circuits for generating a constant current I_o=10 μA. Determine the values of the required resistors assuming that V_{BE} is 0.7 V at a current of 1 mA and neglecting the effect of finite β.

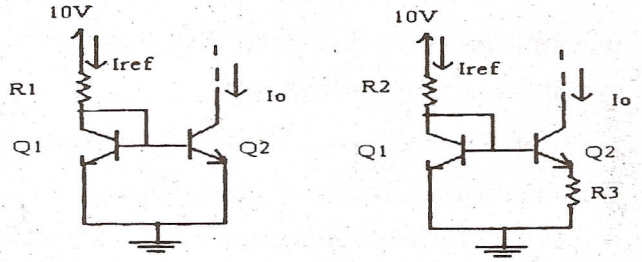

Figure 1

(f) Discuss the Frequency Response of 741 Op-Amp. Relate unity-gain bandwidth (f_t) and Slew Rate (SR).

2. Answer any **four** of the following : **(5×4=20)**

(a) Draw and explain the most commonly used three Op-Amp Instrumentation Amplifier. Also, derive the expression of voltage gain.

(b) Design the high-pass filter at a cutoff frequency of 1 kHz with a passband gain of 2.

(c) Draw and explain Narrow band Reject Filter. Also, find its transfer function.

(d) Design a wide band pass filter with lower cutoff frequency f_L= 200 Hz, higher cutoff frequency f_H=1 kHz and a passband Gain=4.

(e) Derive the expression of voltage gain in KHN Biquad Filter.

(f) Derive the expression for RC Phase Shift Oscillator.

3. Attempt any **two** of the following : **(2×10=20)**

(a) Sketch the Logic gate symbolic representation of clocked SR Flip Flop using nand gates. Also sketch its CMOS circuit implementation and explain its operation.

(b) Draw the D-Flip Flop using CMOS. Also draw and explain its Master slave configuration.

(c) Give the CMOS Logic Circuit that realizes the function of three inputs ODD Parity Checker specifically the Output. is to be high when an odd number (1 or 3) of the input is high.

4. Answer any **two** of the following : **(2×10=20)**

(a) Draw and explain Anti-Log Amplifier. How temperature Compensation is achieved in anti-log amplifier ?

(b) What are Precision rectifiers ? Explain full wave Precision rectifier with necessary waveforms.

(c) Explain :

(i) Schmitt Trigger

(ii) Triangular Wave Generator.

5. Write short notes on any **two** of the following : **(2×10=20)**

(a) (i) R-2R Ladder D/A Converter

(ii) Dual-Slope A/D Converter

(b) 555 Timer as Monostable Multivibrator

(c) Phase Locked Loop and its applications.