(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 2117 Roll No. | | | | | | | | | | |

B. Tech.

(SEMESTER-V) THEORY EXAMINATION, 2012-13

INTEGRATED CIRCUITS

Time : 3 Hours] *[Total Marks : 100*

Section – A

1. Attempt **all** question parts : **10 × 2 = 20**

(a) For Widlar Current source assume the I_{ref} = 1 mA and R_2 = 5 KΩ, neglect base current and find I_{C2}.

(b) List the advantages of Widlar current source.

(c) Find the voltage gain of the CE amplifier with active load circuit when both devices are active.

(d) Define the term "Sensitivity".

(e) Give reason – "The voltage gain of the operational amplifier decreases at high frequencies".

(f) Write some applications of analog multiplier.

(g) What are the parameters determine the performance of VCO ?

(h) Calculate the time period of Astable Multivibrator having $R_1 = R_2$ = 2 KΩ , R = 4 KΩ and C = 0.01 uF.

(i) Why CMOS NAND is preferred over CMOS NOR ?

(j) List the disadvantages of Sallen – Key Unity Gain filter.

Section-B

2. Attempt any **three** question parts : **10 × 3 = 30**

(a) Derive a voltage gain expression for Dual Input Balanced Output Differential Amplifier.

(b) With neat circuit diagram explain the generation of square wave form using Op-Amp astable multivibrator and calculate its total time period.

(c) Design a Wein-Bridge Oscillator circuit and derive expression for sustained oscillations.

(d) (i) Implement the following expression using AOI gate logic.

$$F = \overline{A(B + CD)}$$

(ii) Explain the transistor sizing procedure for a four input NOR gate.

(e) Design a filter using the Sallen – Key unity gain low pass active filter to meet the following specifications: Assume C = 0.027 μf.

(i) Rolloff Rate : 40 dB/decade

(ii) Critical Frequency : 4 kHz

(iii) Pass band as flat as possible

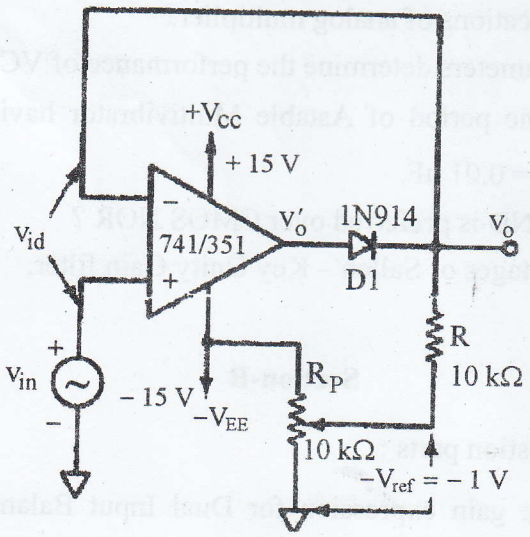
(iv) Gain of 10 at DC

Section – C

Attempt **all** questions : **10 × 5 = 50**

3. Attempt any **two** parts : **5 × 2 = 10**

(a) Draw the output of the following circuit and explain its working.



(b) Draw a Cascode MOS current mirror and calculate its output impedance.

(c) How Current Mirror can be used as an ACTIVE LOAD ? Draw the BJT differential amplifier circuit using ACTIVE LOAD.

4. Attempt any **two** parts : **5 × 2 = 10**

(a) What is the effect of V_0 on I_0 in MOS Current Mirrors ?

(b) Draw and explain sample and hold Op-Amp circuit.

(c) Name the circuit that is used to detect the peak value of the non-sinusoidal waveforms. Explain the operation with neat circuit diagram.

5. Attempt any **two** parts : **5 × 2 = 10**

(a) Two CMOS inverters operating from a 5-V supply have V_{IH} and V_{IL} of 2.42 V and 2.00 V and corresponding outputs of 0.4 and 4.6, respectively, and are connected as a latch. Approximating the corresponding transfer characteristic of each gate by a straight line between threshold points, sketch the latch open-loop transfer characteristic. What are the coordinates of point B (unstable point) ? What is the loop gain at B ?

(b) Draw and explain monostable multivibrator using 555 timer and calculate its time period.

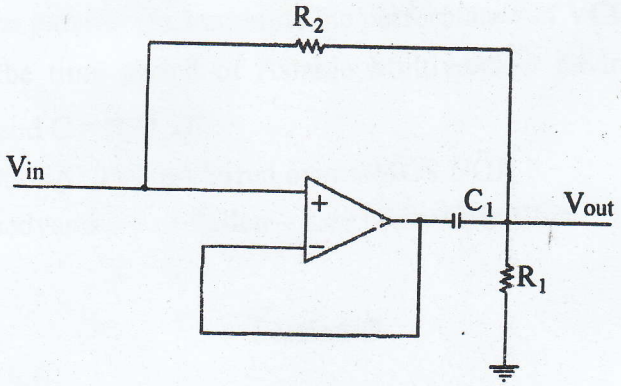
(c) (i) Design a precision peak rectifier and explain its working operation.

(ii) Using a 10 nF capacitor, find the value of R that yields an output pulse of 100 μs in the monostable circuit.

6. Attempt any **one part** : **10 × 1 = 10**

(a) Draw the KHN Biquad filter and derive transfer function of the BPF and LPF from that.

(b) Find the V_{in} / I_{in} for the following circuit :



7. Attempt any **two** parts : **5 × 2 = 10**

(a) Draw and explain the PLL block diagram.

(b) Design a parallel-flash ADC and explain its working.

(c) Draw and explain a GILBERT analog multiplier.
