



(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 131501

Roll No.

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B. Tech.

(SEM. V) (ODD SEM.) THEORY

EXAMINATION, 2014-15

INTEGRATED CIRCUIT

Time : 3 Hours]

[Total Marks : 100

- Note:**
1. Attempt all questions.
 2. All questions carry marks as shown against them

- 1 Attempt any four parts :
- (a) Explain the working of Basic MOSFET current source and current steering circuits. 5
 - (b) Discuss Wilson current mirror and Widlar current source. What are the advantages of Widlar current source over Wilson current mirror? 5
 - (c) Draw the frequency response of IC 741. 5
Give the upper and lower 3dB frequency of same.
 - (d) Define input offset current and input bias current. 5
What is CMRR and virtual ground?

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- (e) Consider a IC 741 having unity gain bandwidth of 1MHz. What maximum gain you can get for an audio amplifier from same IC? 5
- (f) Draw the circuit for anti-log amplifier and derive the expression. 5

2 Attempt any four parts :

- (a) Draw a 4 bit binary weighted D/A converter, find the value of step size if $R=10K$ and $R_f=1.2K$. What is the output voltage when all binary inputs are at 5V? 5
- (b) Design and implement an inverting Schmitt trigger for use as a zero crossing detector with saturation voltages of $\pm 15V$, having hysteresis transition of $\pm 25mV$. 5
- (c) Design and implement a free running astable multivibrator using timer 555 with free running frequency of 5kHz having duty cycle of 30%. 5
- (d) Determine the free running frequency f_{out} and the lock range f_L , and the capture range f_C for PLL 565 having $R_1=12K$, $C_1=0.001\mu F$, $C_2=10\mu F$, $C_3=0.001\mu F$, $V_{cc}=\pm 10V$? Show the graphical representation between lock frequency, capture frequency and free running frequency. 5

- (e) A monostable multivibrator is to be used as divide-by-4 network. The frequency of input trigger is 12 kHz. If the value of $C = 0.05\mu\text{F}$, what should be value of R? 5
- (f) Draw the circuit of KHN filter and derive the expression for its voltage gain. 5

3 Attempt any four parts :

- (a) Sketch a CMOS logic circuit that realizes the function : 5

$$F_1 = ABC + DEF \quad (\text{use only CMOS NOR gate})$$

$$F_2 = (A+B+C).(D+E+F) \quad (\text{use only CMOS NAND gate})$$

- (b) Design a CMOS full adder circuit with inputs A, B, and C and two outputs S and Co. 5
- (c) Sketch the logic gate symbolic representation of SR flip flop using CMOS NAND gates. 5
- (d) Derive the formula for V_{IL} and V_{IH} of CMOS inverter. 5
- (e) Explain the application of PLL as frequency multiplier with suitable circuit diagram. 5
- (f) Explain the types of phase detectors with suitable circuit diagrams and input-output waveforms. 5

4 Attempt any two parts :

- (a) Explain the generation of square and triangular waveforms from astable multivibrator operation using op amp . Also find expression of the time period for both cases. 10

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[Contd...

- (b) (i) How the humming sound or line frequency noise of 50Hz is filtered out? Design and implement active filter for the same. 5
- (ii) What do you understand by precision rectifier? Explain the working of half wave precision rectifier. 5
- (c) Explain the working of dual slope integrating ADC with the help of circuit diagram. 10

5 Attempt any two parts :

- (a) Find expression for V_o in figure 5.1(a). 10

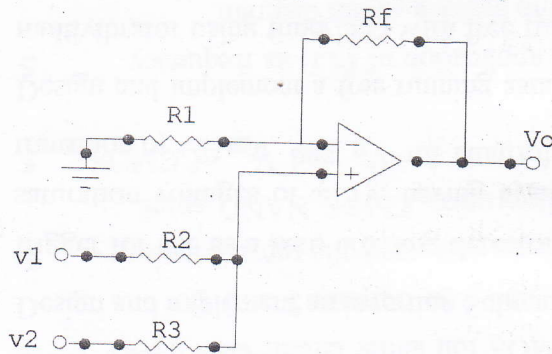


Fig. 5.1(a)

- (b) Design a 2nd order Butterworth high pass filter with overall pass band gain of 3 having corner frequency 2kHz. Also find and plot the frequency response at 100Hz, 500Hz, 1000Hz, 1500Hz, 2000Hz, and 5000Hz. 10
- (c) Design a wide bandpass filter with $f_L = 500\text{Hz}$ and $f_H = 1500\text{Hz}$ and pass band gain of 5, draw frequency response of the filter and find value of Q? 10