

PAPER ID:411027

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**B TECH
(SEM V) THEORY EXAMINATION 2021-22
ADVANCE DIGITAL DESIGN USING VERILOG**

Time: 3 Hours

Total Marks: 100

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

- 1. Attempt all questions in brief. 2 x 10 = 20**
- Explain about the Mixed Logic Circuits.
 - Design the NAND logic gate using 2:1 Multiplexer.
 - What is verilog HDL?
 - What are the major capabilities of verilog HDL?
 - Differentiate between the flip flop and the latch.
 - Define the term Race in Sequential circuits.
 - What do you understand from BDD and OBDD?
 - Explain the term LPDD.
 - Write down the two features of ASIC Logic family.
 - Differentiate between the PLD and CPLD logic family.

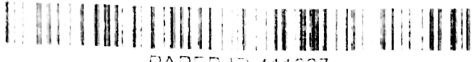
SECTION B

- 2. Attempt any three of the following: 10 x 3 = 30**
- Discuss about the XOR Pattern Handling in brief with the help of suitable example.
 - Design a verilog module for Gray-code counter using file-based task & function and write also its test bench.
 - Discuss about the ASM Charts in brief with the help of suitable example.
 - Explain in detail about the Path Sensitization method with the help of an example.
 - Design the J-K Flip Flop using Complex Programmable Logic Device (CPLD).

SECTION C

- 3. Attempt any one part of the following: 10 x 1 = 10**
- Discuss about the Multiple Output Minimization method with the help of an example.
 - Explain the canonical form and standard form for any boolean function. Also, design the minimum-cost product-of-sums expression for the function:

$$f(x_1, x_2, x_3, x_4) = \sum m(0, 2, 4, 5, 6, 7, 8, 10, 12, 14, 15).$$
- 4. Attempt any one part of the following: 10 x 1 = 10**
- Write a verilog module for Full adder using file-based task & function and write also its test bench.
 - Write a verilog module for half subtractor using file-based task & function and also write its test bench.



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5. Attempt any *one* part of the following: 10 x 1 = 10
- (a) Write short note on:
- i) Multilevel Minimization and Optimization
 - ii) Synchronous State Machines
- (b) Explain in detail about the Asynchronous Sequential Circuit Design using suitable example.
6. Attempt any *one* part of the following: 10 x 1 = 10
- (a) Explain in detail the Boolean Difference Method with the help of an example.
- (b) Explain in detail the Initial State Method with the help of an example.
7. Attempt any *one* part of the following: 10 x 1 = 10
- (a) Discuss the detailed architecture of FPGA logic family with proper diagram.
- (b) Discuss the detailed architecture of PLA logic family with proper diagram.

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