Printed Pages : 4 **TEC-603**

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 3093 Roll No.

B. Tech.

(SEM. VI) EXAMINATION, 2007-08

VLSI TECHNOLOGY AND DESIGN

Time : 3 Hours] *[Total Marks : 100*

Note : *Attempt all questions.*

1 Attempt any four parts of the following : **5×4=20**

(a) Compare BJT, CMOS and Bi-CMOS circuits.

(b) Discuss high frequency model of MOSFET.

(c) Derive the expression for V_{IH}, V_{IL}, NM_L and NM_H for CMOS inverter.

(d) Explain briefly feature size, chips, wafers, hybrid and monolithic circuits.

(e) Discuss CMOS latch up problem.

(f) What are thin film and thick film technology ? Compare them.

2 Attempt any four parts of the following : **5×4=20**

(a) Explain briefly defects in single crystal silicon.

(b) Explain bird's beak enchrochment. How is it minimised ?

(c) Discuss LPCVD process of Si3N4 deposition.

(d) Compare dry and wet process of silicon oxidation. List purposes of oxidation.

(e) Discuss predeposition and drive-in of impurities in silicon.

(f) Draw layout of a CMOS inverter and compare it with static diagram.

3 Attempt any two parts of the following : **10×2=20**

(a) Draw the pull down network for :

$$Y = \overline{A(D+E)+BC}.$$

Also draw pull up network for the above expression using duality. Discuss I-V characteristics of Enhancement and depletion mode devices.

(b) Draw the CMOS VLSI realisation of the EX-OR function using pass transistor logic for two signals. What is the advantage of this realisation ? Discuss design consideration of digital circuits.

(c) Explain how domino CMOS logic is cascadable in VLSI circuit. Also explain MOSFET scaling and small geometry effects .

4 Attempt any two parts of the following : **10×2=20**

(a) Draw and compare three transistors and one transistor dynamic RAM. Explain ROW and column decoder design for RAM.

(b) What is the flash EEPROM ? Discuss briefly tunneling phenomena. Give a comparison of various types of ROM. How power dissipation is reduced in memories.

(c) Compare synchronous counter with asynchronous counter using timing diagram. Discuss static and dynamic sequencing circuits.

5 Attempt any four parts of the following : **5×4=20**

(a) Discuss CPLD applications and compare it with FPGA.

(b) Discuss architecture of FPGA. How FPGA is programmed ?

(c) What are the full custom and semi-custom ASIC? Explain briefly cell based design.

(d) Explain gate array and sea of gates design.

(e) What are stuck-at-zero and stuck-at-one faults ? Explain briefly test and testability of VLSI circuits.

(f) What is BIST? Explain briefly design for testability.
