

(Following Paper ID and Roll No. to be filled in your  
Answer Books)

Paper ID : 121613

Roll No. 1301221160

B.TECH.

Theory Examination (Semester-VI) 2015-16

## INTEGRATED CIRCUITS

Time : 3 Hours

Max. Marks : 100

Note : All Sections are compulsory.

## Section-A

1. All parts are compulsory. Write short answers by giving proper reasons. (2×10=20)

- Sketch the block diagram of op amp IC.
- What do you understand by base current compensated current mirror?
- Draw the generalized impedance convertor circuit.
- Design a filter to remove 240 Hz hum.
- Sketch the CMOS logic circuit realization of the expression:  $Z = \overline{A(B + CD) + E(F + G)}$

(1)

P.T.O.

- (f) Define Fan in and Fan out of digital logic function.
- (g) Explain Peak detector.
- (h) Draw the block diagram of VCO.
- (i) Draw the circuit diagram of flash A/D converter.
- (j) An 8 bit D/A converter has  $V_{ref} = 5$  V. What is the output voltage when  $B_m = 10110100$ ?

### Section-B

Attempt any five parts of the following. [10×5=50]

- (a) Explain Wilson MOS current mirror and derive the expression for output impedance.
- (b) How short circuit protection is achieved? Explain an analysis of gain stage of op amp.
- (c) Design a second order and fourth order low pass filter having upper cut off frequency of 2 kHz. Assume  $C=0.1\mu\text{F}$ .
- (d) What do you mean by analog multipliers? Give any two applications of multiplier.
- (e) Design CMOS logic circuit that realize the EX-OR operation.

(2)

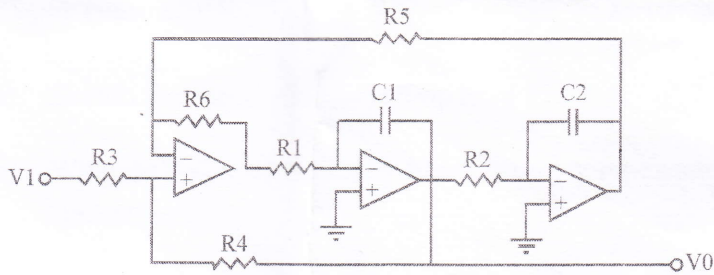
- (f) Explain square wave generator. Also derive the expression of frequency.
- (g) Determine the frequency and duty cycle for 555 astable multivibrator output for  $C = 0.01 \mu\text{F}$ ,  $R_A = 2 \text{K}\Omega$  and  $R_B = 100 \text{K}\Omega$ . Also design astable multivibrator for duty cycle of 50% with same value of capacitor.

### Section-C

Attempt any two parts of the following: (15×2=30)

3. Derive the transfer function of High pass, Low pass & Band pass filter from the given KHN filter as shown in figure.

Assume  $R_1 = R_2 = R_3 = R_4 = R_5 = R_6 = R$  and  $C_1 = C_2 = C$



4. Draw the block diagram of PLL and derive the expression of:
- Lock-in-range
  - Capture range

- (b) What is log and antilog amplifier? Why is it called so? Enlist the disadvantage of simple circuits. Explain modified temperature compensated circuit for both.