B.Tech

(SEM VII) ODD SEMESTER THEORY EXAMINATION 2009-10
DIGITAL SYSTEM DESIGN USING VHDL

Time : 3 Hours] *[Total Marks : 100*

Note : (i) *Attempt **all** questions.*

(ii) ***All** questions carry **equal** marks.*

1 Attempt any **two** parts of the following questions :

10×2

(a) Discuss how VHDL used to describe the behavior and structure of digital system. Explain the following terms (1) VHDL operator, (2) VHDL functions, (3) VHDL, procedure.

(b) Using block diagram explain compilation elaboration and simulation of VHDL code. Write a VHDL description of an SR latch use two logic gates.

(c) Write a VHDL code for a full subtractor using logic equation.

2 Attempt any **two** parts of the following questions :

10×2

(a) Discuss IEEE-1164 standard logic system for use with VHDL.

(b) Explain the various delay provides by VHDL.

(c) Write a short note on synthesis of VHDL codes.

3 Attempt any **two** parts of the following questions :

10×2

(a) Draw a state graph for 4×4 binary multiplier control and discuss the behavioral VHDL model.

(b) Write a high level VHDL description of the divider.

(c) Draw the state graph for faster multiplier and explain the behavioral model for 2's complement multiplier.

4 Attempt any **two** parts of the following questions :

10×2

(a) What is the various floating operation ?
Draw and explain the flow chart for floating point multiplication.

(b) Explain the component of an SM chart. Draw a SM chart for binary multiplier and write the VHDL for SM chart.

(c) Make a one hot state assignment for the state graph of given figure. By inspection, derive the next state and output equations. If a 3000 series FPGA is used, estimate the number of logic cells required to implement the state graph.
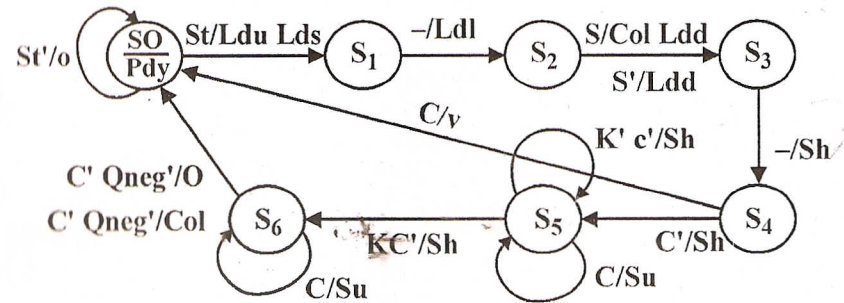

Fig.

5 Attempt any **two** parts of the following questions :

10×2

(a) Design the interfacing between memories of a microprocessor bus.

(b) Explain the simplified block diagram for M68HC05 microcontroller. Explain in brief the various control instruction of 6805 imcrocontroller.

(c) Draw block diagram for UART and SM chart for UART transmitter and discuss the VHDL code for UART transmitter.