(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 2728 Roll No. | | | | | | | | | | |

B.Tech.

(SEM. VII) ODD SEMESTER THEORY EXAMINATION 2012-13

VLSI DESIGN

Time : 3 Hours *Total Marks : 100*

Note :– Attempt **all** the questions. All questions carry equal marks.

1. Attempt any **four** parts : **(5×4=20)**

(a) Draw the Y chart and explain the VLSI design process.

(b) Enlist the classification of CMOS digital logic families. Why CMOS VLSI design is better techniques than its counter parts ?

(c) Explain the concept of regularity, modularity, semi custom and full custom styles of VLSI system design.

(d) What are the various processes of CMOS fabrication ? Illustrate the main steps in a typical n-well process.

(e) Explain the scaling down of MOS-Transistor using Constant Field Scaling and its limitation.

(f) Explain symbol, different colours and lines used for drawing stick diagram. Draw a stick diagram of CMOS inverter.

2. Attempt any **two** parts : **(10×2=20)**

(a) Measured voltage and current data for a MOSFET are given below :

V_{GS}(V)	V_{DS}(V)	V_{SB}(V)	I_D(μA)
3	3	0	97
4	4	0	235
5	5	0	433
3	3	3	59
4	4	3	173
5	5	3	347

Determine the type of the device and calculate the parameters k_n V_{T0} and γ. Assume $\phi_F = -0.3V$.

(b) Consider a CMOS inverter circuits with the following parameters $V_{DD} = 3.3V$, $V_{Ton} = 0.6V$, $V_{Top} = -0.7V$, $\mu_n C_{ox} = 60\ \mu A/V^2$, $(W/L)_n = 8$, $\mu_p C_{ox} = 20\ \mu A/V^2$, $(W/L)_p = 12$. Calculate the noise margin of the circuits.

(c) Consider a CMOS inverter, with the following device parameters, $V_{DD} = 5V$, $V_{Ton} = 0.8V$, $V_{Top} = -1.0V$, $\mu_n C_{ox} = 50\ \mu A/V^2$, $\mu_p C_{ox} = 20\ \mu A/V^2$, $\lambda = 0$. Both transistor have a channel length of $L_n = L_p = 1\ \mu m$. The total output load capacitance of this circuit is $C_{out} = 2pF$, which is independent of transistor dimensions.

(i) Determine the channel width of the nMOS and the pMOS transistors such that the switching threshold voltage is equal to 2.2V and the output rise time $\tau_{rise} = 5ns$.

(ii) Calculate the average propagation delay time τ_p.

3. Attempt any **two** parts : **(10×2=20)**

(a) Consider the logic circuit shown in Figure 1 with V_{TO}(enhancement) = 1V and V_{TO}(depletion) = –3 V and $\gamma = 0$.

(i) Determine the logic function F

(ii) Calculate WL/LL such that VOL does not exceed 0.4V. Explain the behaviour of Pass transistor in dynamic CMOS logic implementation.

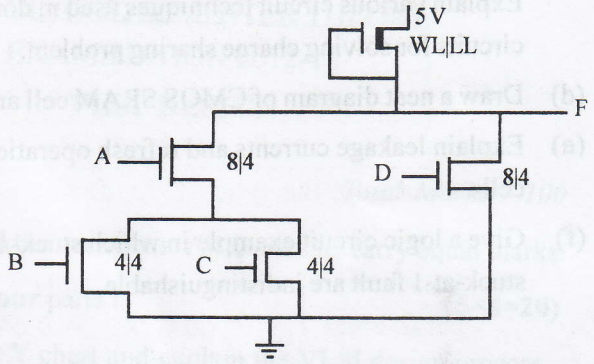

Figure 1

(b) Explain the behaviour of Pass transistor in dynamic CMOS logic implementation. With a neat schematic diagram, explain SR flip-flop implementation using pass transistor logic.

(c) Design the circuit described by the Boolean function $Y = \overline{A \cdot (B + C)(D + E)}$ using CMOS logic. Calculate the equivalent CMOS inverter circuit for simultaneous switching of all inputs assuming that $\left[\frac{W}{L}\right] = 5$ for pMOS transistor and $\left[\frac{W}{L}\right] = 2$ for all nMOS transistor.

4. Attempt any **four** parts : **(5×4=20)**

(a) Draw a 4 × 1 multiplexer using Transmission Gate (TG).

(b) Enlist the classification of dynamic CMOS logic circuit and discuss the advantage of dynamic logic circuit over static CMOS logic circuit.

(c) Discuss the charge sharing problem in VLSI circuits. Explain various circuit techniques used in domino CMOS circuits for solving charge sharing problem.

(d) Draw a neat diagram of CMOS SRAM cell and explain it.

(e) Explain leakage currents and refresh operation in DRAM cells.

(f) Give a logic circuit example in which stuck-at-0 fault and stuck-at-1 fault are indistinguishable.

5. Attempt any **four** parts : **(5×4=20)**

(a) Discuss the various design techniques involved in low power CMOS VLSI circuits.

(b) Write a short note on Adiabatic logic circuit.

(c) Explain the different kinds of Physical defect (faults) that can occur on a CMOS circuits.

(d) Define the terms Controllability and Obervability.

(e) Discuss in brief Ad-Hoc Testable design techniques.

(f) Write a short note on Buit-in-self test (BIST) techniques.