(Following Paper ID and Roll No. to be filled in your Answer Book)											
PAPER ID: 2721	Roll No.		0	0	3	2	2	1	0	7	Ż

## B. Tech.

## (SEM. VII) ODD SEMESTER THEORY EXAMINATION 2013-14

## EMBEDDED SYSTEM

Time: 3 Hours

Total Marks: 100

Note: - (i) Answer all questions.

- (ii) All questions carry equal marks.
- 1. Attempt any four parts of the following:

 $(5 \times 4 = 20)$ 

- (a) Draw and explain the block diagram of a two level bus architecture in a microprocessor based embedded system.
- (b) How does concurrent processing help in VLIW instruction execution at high speed?
- (c) Explain the need of watchdog timer.
- (d) What are the advantages offered by an ASIP for designing an embedded system?
- (e) Explain use of each control bit of I<sup>2</sup>C bus.
- (f) How does memory allocation differ in RTOS and OS? What is memory locking?
- 2. Attempt any two parts of the following:

 $(10 \times 2 = 20)$ 

(a) Discuss the advantages and disadvantages of using memory-mapped I/O versus standard I/O mapped.

EEC047/DNG-51961

[Turn Over

- (b) Define Harvard and Von Neumann architecture and what are the advantages of Harvard architecture?
- (c) How does a decoder help in memory and I/O devices interfacing? Draw Four Exemplary circuit.
- 3. Attempt any two parts of the following:  $(10 \times 2 = 20)$ 
  - (a) Describe Pipelining, Superscalar and VLIW Architectures.
  - (b) What is interrupt vector? Determine the contents of the Accumulator after the execution of the following program segments:

MOV A, #3CH

MOV R4, #66H

ANLA, R4

- (c) Write ARM instruction for the following Z=(a<2)| (b&15)
- 4. Attempt any two parts of the following:  $(10 \times 2 = 20)$ 
  - (a) Discuss the advantages and disadvantages of using memory-mapped I/O versus standard I/O mapped. Explain the direct mapping techniques for cache.
  - (b) Write a short note on hierarchical RTOS. List three ways in which an RTOS handles the ISRs in a multitasking environment.
  - (c) Draw and explain serial transmission using UART's, a PC communicating serially with an embedded device.
- 5. Attempt any two parts of the following:  $(10 \times 2 = 20)$ 
  - (a) Describe Pipelining and Superscalar architectures. Write the differences between RISC and CISC.
  - (b) Draw system architecture of DMA using the ISA bus protocol and explain its memory write bus cycle.
  - (c) Write difference between 8051 Microcontroller and Microprocessor and write a program that will produce an output at port0 that counts down from 80H to 00H.

625