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(Following Paper ID and Roll No. to be filled in your Answer Book)

Paper ID : 131703 | Roll No. | | | | | | | | | |

B.Tech.

(SEM. VII) THEORY EXAMINATION, 2015-16

VLSI DESIGN

[Time:3 hours] **[Total Marks:100]**

Section-A

1. Attempt **all** parts. All parts carry equal marks. Write answer of each part in short. (2x10=20)

   (a) Why leakage power dissipation has become an important issue in deep submicron technology in deep submicron technology?

   (b) How the latch up problem can be overcome?

   (c) Distinguish between the bulk CMOS technology with the SoI technology fabrications.

   (d) What is body effect? How does it influence the threshold voltage of a MOS transistor?

(e) Distinguish between constant field and constant voltage feature size scaling? Compare their advantages and disadvantages.

(f) How does the ON-resistance of a transmission gate changes as the input varies from 0 V to V_{dd}, when the output has a light capacitive load.

(g) What are the various ways to reduce the delay time of a CMOS inverter ?

(h) How the limitations of a ROM based realization is overcome in a PLA-based realization.

(i) Explain the basic operation of a 2-phase dynamic circuit?

(j) What is charge leakage problem of dynamic CMOS circuits? How is it overcome?

Section-B

Attempt **any five** Questions from this section. (10×5=50)

2. Draw the Y-Chart and explain the VLSI design process.

3. Derive and explain the working of CMOS inverter with its VTC characteristics. Also calculate the V_{OL}, V_{OH}, V_{IL}, V_{IH} and V_{TH} for the CMOS inverter.

4. Draw and explain the working of CMOS negative edge triggered Master slave D-flip flop.

5. Compare the performance of Domino CMOS logic and NP-Domino CMOS logic with suitable example.

6. Explain the working of Three - transistor D-RAM cell with concept of leakage currents and refresh operation. What are the features required to select a proper RAM.

7. Discuss the classification of CMOS digital logic families.

8. Explain the following :

   a) Explain the behavior of bistable elements. Explain the working of CMOS NOR based clocked JK latch.

   b) Draw a 4×1 Multiplexer using transmission gate.

9. Explain the following :

   a) Controllability and observability.

   b) Explain the implementation of Built-In Self Test (BIST) design techniques for VLSI circuit testing.

Section-C

Attempt **any two** questions from this section. (15x2=30)

10. Derive the expression for fall time and rise time for CMOS inverter.

11. Explain the working of pass transistor circuit. Also explain how the charge stored affects the transfer of logic "I" and logic "O" in NMOS pass transistor circuits.

12. Explain the techniques used in designing the low power CMOS logic circuits.

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