PAPER ID-310615

Roll No: | | | | | | | | | | | | | |

B.TECH
(SEM-VII) THEORY EXAMINATION 2020-21
VLSI Design

Time: 3 Hours ***Total Marks: 70***

Note: Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. 2 x 7 = 14

Q no	Question	Marks	CO
a.	State Moore's law in reference to VLSI design.	2	1
b.	Implement EX-OR gate using CMOS logic.	2	1
c.	Differentiate between Static power and Dynamic power.	2	2
d.	Define the term Interconnect impact in brief.	2	3
e.	Mention the advantages of dynamic logic circuits over static logic circuits?	2	4
f.	Comment on overview of power consumption in CMOS logic circuits.	2	5
g.	Define the term interconnect delay.	2	2

SECTION B

2. Attempt any *three* of the following: 7 x 3 = 21

Q. no	Question	Marks	CO
a.	Explain the CMOS fabrication steps with neat diagram using n-well process.	7	1
b.	Explain RC delay model for interconnects.	7	2
c.	Implement the Boolean expression Y=AB+(C+D)(E+F)+(G+H)	7	4
d.	Mention the advantages of interconnect modeling. Describe the interconnect modeling to calculate R and C.	7	3
e.	Discuss the various design techniques involved in low power CMOS VLSI circuits.	7	5

SECTION C

3. Attempt any *one* part of the following: 7 x 1 = 7

Q no.	Question	Marks	CO
a.	Draw the Y chart and explain the VLSI design process. Mention its advantages.	7	1
b.	Explain symbol, different colors and lines used for drawing stick diagram. Draw the Stick diagram of CMOS inverter.	7	1

4. Attempt any *one* part of the following: 7 x 1 = 7

Q no.	Question	Marks	CO
a.	Define the term Logical effort & Electrical effort. Explain Linear RC delay model. Mention the limitation of this model.	7	2
b.	Explain the Elmore delay model with suitable RC networks. Mention its merits.	7	2

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5. Attempt any *one* part of the following: 7 x 1 = 7

Q no.	Question	Marks	CO
a.	Define the term Energy delay product (EDP) and Power delay product (PDP). Describe different low power architectures with suitable diagrams.	7	3
b.	Explain the interconnect Engineering in detail.	7	3

6. Attempt any *one* part of the following: 7 x 1 = 7

Q no.	Question	Marks	CO
a.	What is SRAM? Explain CMOS SRAM cell design strategy.	7	4
b.	Explain the behavior of Pass transistor in dynamic CMOS logic implementation.	7	4

7. Attempt any *one* part of the following: 7 x 1 = 7

Q no.	Question	Marks	CO
a.	Explain the term Controllability and Observability in detail.	7	5
b.	With the help of suitable diagram, Explain Scan based technique.	7	5