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TEC – 042

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 0392 Roll No. | | | | | | | | | | |

B.Tech.

(SEM VIII) EVEN SEMESTER THEORY EXAMINATION, 2009-2010

VLSI DESIGN

Time : 3 Hours *Total Marks : 100*

Note : *(i) Attempt **ALL** questions.*

(ii) Assume the missing data if any.

*(iii) All questions carry **equal** marks.*

1. Attempt **any four** parts of the following : **(4x5=20)**

(a) Define the term Pull-up and Pull-down network (PUN/PDN) used in an inverter circuit. Will NMOS or PMOS alone be used for PUN as well as PDN ? Give reasons in support of your answer.

(b) Explain the difference between polycide and salicide CMOS process. Which would be likely to have higher performance and why ?

(c) List the parameters that affect the threshold voltage of a MOS transistor. What is the effect of high-k dielectric when used instead of SiO_2 in MOSFET ?

(d) Which polysilicon gates (n^+ or p^+) are preferred and why ? Does the present technology require palysilicon as replacement of metal gates ?

(e) In which region of I-V characteristics the MOSFET simply acts like a resistor ? How does the gate voltage modify its resistivity ?

(f) Discuss the important features of Lambda based design rules.

2. Attempt **any two** parts of the following : **(2x10=20)**

(a) Discuss the role of scaling in the development of VLSI. Differentiate between constant voltage scaling and constant field scaling. In both scaling technique what effects are seen in the electrical performance of the device.

(b) Implement the function 'F' given below by CMOS gates. Also draw its stick diagram :

$$F = \left(E + \overline{D}\right) . \left(\overline{A} . D + \overline{B} . \left(A + \overline{C}\right)\right)$$

(c) Compare the pass-transistor logic circuit with that of transmission gates. Implement 8 to 1 MUX circuit using CMOS transmission gates and explain its working.

3. Attempt **any two** of the following : **(2x10=20)**

(a) Explain the operation of BICMOS inverter circuit. Compare its performance with that of a CMOS inverter circuit (Noise - Margin, Response Speed and Power Consumption)

(b) Draw and explain the VTC curve of NMOS inverter using enhancement load - Also show its stick diagram.

(i) If input voltage falls from high to low what changes are seen in the working of driver and load transistor ?

(ii) How fall can be improved in such types of inverter circuit ?

(iii) Why depletion loads is preferred compared to enhancement load ?

(c) Classify ASICs. Compare their performanceses. How a fixed part costs associated with ASIC design can be calculated ?

4. Attempt **any two** of the following : **(2x10=20)**

(a) Discuss the strategy for developing manufacturable specifications for chip processing in terms of required control on threshold voltages, variations in channel lengths and widths, gate oxide thickness, and substrata and tub doping profiles.

(b) Explain the merits or demerits of the bus structure in relation to testability. How would the bus structure impact the chip overhead ?

(c) Give a logic circuit example in which stuck-at-1 fault and stuck-at-0 fault are in-distinguishable. Show a few logic circuit examples whose logical fault coverage is dependent on the test vector sequence.

5. Write short notes on **any two** of the following : **(2x10=20)**

(a) Serial-Scan Testing

(b) BIST

(c) 6T SRAM cell

(d) Domino Logic "Circuit"

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