PAPER ID-311738

Subject Code: KCS302

Roll No: | | | | | | | | | | | | | |

BTECH

(SEM III) THEORY EXAMINATION 2023-24

COMPUTER ORGANIZATION AND ARCHITECTURE

TIME: 3HRS **M.MARKS: 100**

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief.

Q no.	Question	Marks
a.	Define Computer organization and architecture.	2
b.	Draw the basic functional units of a computer.	2
c.	Explain non-restoring method in division algorithm.	2
d.	What is the role of Multiplexer and Decoder	2
e.	Write the difference between RISC and CISC.	2
f.	Define the term Program control.	2
g.	Define hit ratio.	2
h.	Define Locality of reference.	2
i.	Explain the term burst stealing.	2
j.	Differentiate between Horizontal & Vertical microprogramming.	2

SECTION B

2. Attempt any *three* of the following:

a.	Define various methods of Bus arbitration with their advantages and disadvantages.	10
b.	Explain IEEE standard for floating point representation. Represent the number (-65.175)10 in single and double precision format.	10
c.	What is micro program sequencer? With block diagram, explain the working of micro program sequencer.	10
d.	Digital computer has a memory unit of 64K X 16 and a cache memory of 1K words. The cache uses direct mapping with block size of four words. Evaluate the following- (i). Number of bits in tag, index, block and word fields of the address format. (ii). Number of bits in each word of cache, and how they are divided into functions? Include a valid bit. (iii). No of blocks can the cache accommodate.	10
e.	What do you mean by asynchronous data transfer? Explain strobe control and hand shaking mechanism.	10

SECTION C

3. Attempt any *one* part of the following:

a.	A bus-organized CPU has 16 registers with 32 bits in each. an ALU, and a destination decoder. a) How many selection Inputs are needed for MUX A and MUXB? b) How many inputs and outputs are there in the ALU for data, including input and output carries? c) Calculate a control word for the system if the ALU has 35 operations. d) How many inputs and outputs are there in the decoder? e) How many multiplexers are there In the A bus, and what is the size of each multiplexer?	10

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b.	Explain General Register Organization with the help of suitable diagram.	10

4. Attempt any *one* part of the following:

a.	Explain the flow chart of Booth's Algorithm for multiplication and show the multiplication process using Booth's Algorithm for (-9) X (+13).	10
b.	Explain in detail the principle of Carry looks ahead adder and design 4-bit CLA adder.	10

5. Attempt any *one* part of the following:

a.	What is pipelining in computer Architecture? Also discuss its various types.	10
b.	Differentiate between RISC and CISC.	10

6. Attempt any *one* part of the following:

a.	Discuss different types of auxiliary memories.	10
b.	Evaluate the page fault for the given string with the help of LRU & FIFO page replacement algorithm, Size of the frames = 4 and string 2 3 1 4 2 1 5 6 2 1 3 1 6 67 3 2 1 2 3 6.	10

7. Attempt any *one* part of the following:

a.	Explain the working of DMA controller with help of suitable diagrams.	10
b.	What are interrupts? How are they handled?	10