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BTECH
(SEM III) THEORY EXAMINATION 2023-24
DIGITAL LOGIC DESIGN

TIME: 3HRS

M.MARKS: 70

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt all questions in brief. 2 x 7 = 14

a.	Implement XOR logic using only NAND Gates.
b.	Write the difference between combinational and sequential circuits.
c.	Convert the decimal number 512786 in Excess-3 code.
d.	Explain the difference between latch and flip flop.
e.	State and prove DE Morgan's theorem.
f.	Differentiate between synchronous and asynchronous sequential circuits.
g.	Differentiate between PLA and PAL.

SECTION B

2. Attempt any three of the following: 7 x 3 = 21

a.	Demonstrate following Boolean function $F = \sum m(1,3,7,11,15) + d(0,2,4)$ by using K-map method and obtain a) Minimal SOP and b) Minimal POS expression
b.	Demonstrate the BCD adder circuit.
c.	Illustrate race around condition in sequential circuits.
d.	Discuss CMOS as inverter circuit.
e.	Explain the working of DTL and ECL with suitable diagram.

SECTION C

3. Attempt any one part of the following: 7 x 1 = 7

(a)	Minimize $F = \sum m(0,2,3,7,5,8,10,11,14,15)$.
(b)	Encode the binary word 1010 into a 7-bit even parity Hamming code.

4. Attempt any one part of the following: 7 x 1 = 7

(a)	Design a full adder by constructing the truth table and simplify the output equations.
(b)	Illustrate 3 bit encoder with truth table and block diagram.

5. Attempt any one part of the following: 7 x 1 = 7

(a)	Design MOD 4 synchronous counter using T FF.
(b)	Design MOD 3 asynchronous counter using JK flip flop.

6. Attempt any one part of the following: 7 x 1 = 7

(a)	Design a sequence generator using D-Flip Flop to generate the sequence 10110.
(b)	Illustrate the block diagram of asynchronous sequential circuits and explain the different steps for analysis of asynchronous sequential circuits.

7. Attempt any one part of the following: 7 x 1 = 7

(a)	Explain R to 2R ladder type digital to analog converter with a neat sketch.
(b)	Explain single slope and dual slope ADC with a neat sketch.