PAPER ID-311323

Subject Code: KOE039

Roll No: | | | | | | | | | | | | | |

BTECH
(SEM III) THEORY EXAMINATION 2023-24
DIGITAL ELECTRONICS

TIME: 3HRS **M.MARKS: 100**

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x 10 = 20**

Q no.	Question	Marks	CO
a.	Convert the decimal number 25 into its binary equivalent.	2	1
b.	Perform the addition of the binary numbers 1011 and 1101.	2	1
c.	Define MSI devices.	2	2
d.	Describe the operation of a decoder.	2	2
e.	Define latches and flip flops.	2	3
f.	Write the applications of shift registers.	2	3
g.	Define synchronous and asynchronous sequential circuits.	2	4
h.	Explain the concept of state machine design in digital circuit.	2	4
i.	Define noise margin in logic family.	2	5
j.	Differentiate between RAM and ROM.	2	5

SECTION B

2. Attempt any *three* of the following: **10 x 3 = 30**

a.	Explain in details decimal system and binary systems with examples.	10	1
b.	Explain the difference between a half adder and a full adder. Provide truth tables for both.	10	2
c.	Design a 4-bit shift register using D flip flops.	10	3
d.	Explain the key steps involved in state reduction and state assignment for synchronous sequential circuits.	10	4
e.	Define the following digital logic families: DTL, DCTL, TTL, ECL, and CMOS. Discuss their characteristics and applications.	10	5

SECTION C

3. Attempt any *one* part of the following: **10 x 1 = 10**

a.	Derive the Sum Of Products (SOP) and Product Of Sums (POS) forms for the Boolean function F(A, B, C) = Σ(1, 3, 5, 7). Use Karnaugh maps to simplify both forms	10	1
b.	Briefly describe the Quine-McClusky tabular method for minimizing multiple-output logic functions.	10	1

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4. Attempt any *one* part of the following: 10 x 1 = 10

a.	Explain the operation of a BCD adder and its significance in digital arithmetic.	10	2
b.	Explain the working principle of a 4-bit magnitude comparator using truth tables and logic diagrams.	10	2

5. Attempt any *one* part of the following: 10 x 1 = 10

a.	Explain the concept of a ripple counter. Provide an example of a 3-bit ripple counter.	10	3
b.	Describe the working principle of synchronous counters and their advantages over ripple counters.	10	3

6. Attempt any *one* part of the following: 10 x 1 = 10

a.	Describe the procedure for reducing state table and flow table in asynchronous circuits.	10	4
b.	Explain the design procedure of clocked sequential circuits.	10	4

7. Attempt any *one* part of the following: 10 x 1 = 10

a.	Discuss the advantages and disadvantages of TTL, ECL & CMOS digital logic family in terms of speed, power consumption, and noise immunity.	10	5
b.	Explain the operation of a Programmable Logic Array (PLA) with example.	10	5