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BTECH
(SEM V) THEORY EXAMINATION 2024-25
VLSI TECHNOLOGY

TIME: 3 HRS**M.MARKS: 70****Note:** Attempt all Sections. In case of any missing data; choose suitably.**SECTION A****1. Attempt all questions in brief. 2 x 07 = 14**

Q no.	Question	CO	Level
a.	What is ingot?	CO1	K1
b.	Differentiate between homo epitaxy and hetero epitaxy.	CO2	K1
c.	List the Figures of Merit in photolithographic process.	CO3	K2
d.	Name the etchant commonly used to remove Silicon.	CO3	K2
e.	Name any two solid sources for n-type dopant sources.	CO4	K1
f.	Write the advantage of using Aluminium in metallization.	CO5	K1
g.	Define throughput for IC fabrication.	CO5	K1

SECTION B**2. Attempt any three of the following: 07 x 3 = 21**

a.	Compare FZ and CZ Technique for crystal growth. Explain evaluation of crystal.	CO1	K2
b.	Explain the basic transport processes and reaction kinetics of Vapor Phase Epitaxy.	CO2	K2
c.	Define photolithography. Discuss the steps of mask generation with diagram.	CO3	K2
d.	Explain Models for Diffusion in Solids. Also explain Fick's I Law of Diffusion.	CO4	K2
e.	Write short notes on (i) Sputtering (ii) Applications of Metallization	CO5	K2

SECTION C**3. Attempt any one part of the following: 07 x 1 = 07**

a.	Explain the different steps involved in shaping of Silicon wafers.	CO1	K2
b.	Why Oxidation is necessary in IC fabrication? Compare High pressure oxidation and Plasma oxidation.	CO1	K2

4. Attempt any one part of the following: 07 x 1 = 07

a.	Explain Molecular Beam Epitaxy with diagram. Also discuss the advantages and disadvantages of Molecular Beam Epitaxy.	CO2	K2
b.	Write short notes on (i) Pre-oxidation Cleaning (ii) Wet Oxidation	CO2	K2

5. Attempt any one part of the following: 07 x 1 = 07

a.	Explain the deposition methods and deposition variables for Silicon Dioxide. Explain step coverage problem in Silicon Dioxide deposition.	CO3	K2
b.	Write short notes on (i) Wet Etching (ii) Projection Printing	CO3	K2

6. Attempt any one part of the following: 07 x 1 = 07

a.	Explain the ion-implantation technique with diagram of equipment. Discuss the advantages and disadvantages of ion-implantation.	CO4	K2
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b.	Derive an expression for complementary error function (erfc) diffusion profile.	CO4	K2
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7. Attempt any one part of the following: 07 x 1 = 07

a.	Explain CMOS fabrication process sequence using twin-well technology with diagrams.	CO5	K2
b.	What is the need of packaging in VLSI? Discuss Packaging Design considerations in VLSI.	CO5	K2

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