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BTECH
(SEM V) THEORY EXAMINATION 2024-25
INTEGRATED CIRCUITS

TIME: 3 HRS

M.MARKS: 70

Note: Attempt all Sections. In case of any missing data; choose suitably.

SECTION A

1. Attempt all questions in brief.

2 x 07 = 14

Q no.	Question	CO	Level
a.	Write the limitations of integrated circuits.	1	1
b.	Draw a non-inverting amplifier with voltage gain of 5.	1	1
c.	State the applications of V to I converter and I to V converter.	2	2
d.	Define notch filter.	2	1
e.	List the applications of sample and hold circuit.	3	1
f.	Explain CMOS circuit logic.	4	2
g.	Define lock-in & capture range of PLL.	5	1

SECTION B

2. Attempt any three of the following:

07 x 3 = 21

Q no.	Question	CO	Level
a.	Calculate the overall voltage gain provided by IC 741 after drawing the small signal models of each stage.	1	
b.	Derive the expression of voltage gain in KHN Biquad Filter. Draw the KHN Biquad filter and derive the transfer function of the BPF and LPF from KHN Biquad filter.	2	K3
c.	Explain in detail about the methods of frequency compensation used in operational amplifiers.	3	K2
d.	Sketch the CMOS logic circuit implementation of the given expression: $Y = (A + B)C + DE$	4	K3
e.	Draw and explain the working principle of op-amp based voltage controlled oscillator circuit.	5	K2

SECTION C

3. Attempt any one part of the following:

07 x 1 = 07

Q no.	Question	CO	Level
a.	How the short circuit protection is achieved in the output stage of 741 op-amp? Draw and explain the frequency response of IC 741.	1	K2
b.	Explain Wilson current mirror and Widlar current source with circuit diagram. Also discuss advantages of Widlar current source.	1	K2

4. Attempt any one part of the following:

07 x 1 = 07

Q no.	Question	CO	Level
a.	Explain the principle of Instrumentation amplifier and derive the gain for that circuit. Give its applications.	2	K2
b.	Explain the operation of a triangular wave generator by drawing the capacitor and output voltage waveforms.	2	K2

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5. Attempt any one part of the following: 07 x 1 = 07

Q no.	Question	CO	Level
a.	Explain in detail about the methods of frequency compensation used in operational amplifiers.	3	K2
b.	Derive expression for log and anti-log amplifiers with diagrams.	3	K2

6. Attempt any one part of the following: 07 x 1 = 07

Q no.	Question	CO	Level
a.	Sketch CMOS implementation of J-K Flip-flop and explain its operation. Also discuss the limitations of J-K flip flop.	4	K2
b.	Realize following 2 input logic gates using CMOS (i) NAND (ii) EX-OR (ii) NOR	4	K2

7. Attempt any one part of the following: 07 x 1 = 07

Q no.	Question	CO	Level
a.	(i) Draw the circuit of monostable multivibrator using IC 555 timer. (ii) Design an astable multivibrator using 555 timer to provide an output signal frequency of 2 KHz and 75 % duty cycle with block diagram. (Consider $C=0.1\mu\text{F}$)	5	K3
b.	Explain with a schematic how a PLL can be used as (i) Frequency multiplier (ii) Frequency translator.	5	K2