(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 1471 Roll No. | | | | | | | | | | |

MCA

SECOND SEMESTER EXAMINATION, 2005-2006

COMPUTER ARCHITECTURE AND MICROPROCESSOR

Time : 3 Hours *Total Marks : 100*

Note : *(i) Attempt ALL questions.*

(ii) All questions carry equal marks.

(iii) In case of numerical problems assume data wherever not provided.

(iv) Be precise in your answer.

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1. Attempt ***any two*** parts of the following : **(10x2=20)**

(a) Discuss various architectural of parallel computer classification scheme.

(b) In the following block of computations, a and b are two external inputs and z in the final output. Two intermediate results are labelled x and y.

$x \leftarrow a*a\ ;\ y \leftarrow b*b\ ;\ z \leftarrow (x+y)/(x-y)$

(i) Draw a data flow graph for this code block, where $*, +, -$, and / are arithmetic operators.

(ii) Show a template implementation of the data flow graph in (i)

(iii) Indicate the events that can be done in parallel in the execution of the above block of codes.

(c) Formulate a six-segment instruction pipeline for a computer. Specify the operations to be performed in each segment.

2. Attempt *any two* parts of the following : **(10x2=20)**

(a) Describe the following terminologies associated with pipeline computers and vector processing.

(i) Unifunctional and Multifunctional pipeline

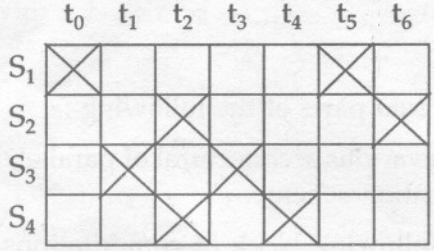
(ii) Pipeline efficiency and throughout

(iii) Simple and Greedy cycle

(iv) Data dependent hazards

(v) Vectorizer

(b) A certain dynamic pipeline with the four segments S_1, S_2, S_3 and S_4 is characterized by the following reservation table :



(i) Determine latencies in the forbidden list F and the collision vector C.

(ii) Determine the minimum constant latency L by checking the forbidden list.

(iii) Draw the state diagram for this pipeline. Determine the minimal average latency (MAL) and the maximum through put of this pipeline.

(c) Answer the following which is related to the task initiation cycle (2, 3, 7) for a given pipelined processor :

(i) What are the period p and the average latency la of the initiation cycle ?

(ii) Specify the initiation internal set G (mod p).

(iii) What is the necessary and sufficient condition that a given task initiation cycle is allowed by a pipeline with a forbidden latency set F ?

3. Attempt *any two* parts of the following : **(10x2=20)**

(a) In case of SIMD interconnection network, explain the following :

(i) Static versus dynamic network

(ii) Cube Interconnection network

(b) Explain the SIMD matrix multiplication.

(c) Explain the following :

(i) Shuffle - Exchange network

(ii) Omega Network.

4. Attempt *any two* parts of the following : **(10x2=20)**

(a) Explain the following :

(i) Loosely coupled Microprocessors

(ii) Tightly coupled Microprocessors.

(b) In case of multiprocessor scheduling strategies, explain the Deterministic Scheduling Model for scheduling scheme.

(c) (i) Show instruction execution in a dataflow computer for the computation of $a=(b+1)*(b-c)$

(ii) Explain a static dataflow computer organisation and dynamic data flow computer organisation.

5. Attempt *any four* parts of the following : (5x4=20)

(a) What is a transparent latch, and why is it necessary to use a latch with output devices such as LEDs ?

(b) Explain the functions of ALE and IO/$\overline{M}$ signals of the 8085 microprocessor.

(c) List the four categories of 8085/8080 A instructions that manipulate data.

(d) Write a program using the ADI instruction to add the two hexadecimal numbers 3AH and 48 H, and to display the answer at an output port.

(e) Write a program to add the following five data bytes stored in memory locations starting at 2060 H. If the sum generates a carry, stop the addition, and display 01 H at the output port. Otherwise, continue adding and display the sum. Data (H) 98, A2, 39, 22, 42.

(f) Write a program to control a railway crossing signal that has two alternately flashing red lights, with a 1- second on time for each light.

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