



Printed Pages : 4

MCA-206

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 1471

Roll No.

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M.C.A.

(SEM. II) EXAMINATION, 2007-08
COMPUTER ARCHITECTURE &
MICROPROCESSOR

Time : 3 Hours]

[Total Marks : 100

- Note :**
- (1) Attempt **all** questions. All questions carry **equal** marks.
 - (2) Assume suitable missing data and specify it clearly.

1 Attempt any **two** parts of the following : **10×2=20**

- (a) Explain the Flynn's classification of computer architectures by showing their block diagrams.
- (b)
 - (i) If there are no hazards of any kind, what is the average CPI of 100 instructions moving through 5-stage pipelined processor.
 - (ii) Derive speedup, efficiency and throughput of a linear k-stage pipeline to process n tasks with τ as the clock period.
- (c)
 - (i) Discuss various architectural features of a parallel computer classification scheme. How do we compare performance of various parallel architectures.
 - (ii) Explain the role of data flow graphs in parallel computing.



Attempt any **two** parts of the following :

$10 \times 2 = 20$

(a) Consider the five-stage pipelined processor specified by the following reservation table :

	1	2	3	4	5	6
S_1	X					X
S_2		X			X	
S_3			X			
S_4				X		
S_5		X				X

- (i) Draw a state transition diagram showing all possible initial sequences without causing a collision in the pipeline.
 - (ii) Identify the greedy cycles among the simple cycles.
 - (iii) What is the minimum average latency of this pipeline ? Is it optimal ? If not, how can you improve it ?
 - (iv) Let the pipeline clock period be $\tau = 20$ ns. Determine the throughput of this pipeline.
- (b) Explain the following memory organizations for vector access :
- (i) S-access memory organization
 - (ii) C-access memory organization.
- (c) Explain the following in brief : (any **four**)
- (i) Effect of clock skewing in pipelined processors.
 - (ii) Asynchronous and synchronous pipeline models



- (iii) Vectorizer
- (iv) Hazard resolution techniques
- (v) Internal data forwarding.

3 Attempt any **two** parts of the following : **10×2=20**

- (a) (i) What are the major advantages and disadvantages of the crossbar switching networks and the bus-based networks.
- (ii) Compare the tightly and loosely coupled multiprocessors.
- (b) (i) Show the recursive construction of a 16×16 baseline network.
- (ii) Define the terms : Node degree, Network Diameter, Bisection width, Network latency, Broadcast Networks.
- (c) Show the node interconnection diagram for cube networks in both static topology and multistage dynamic network topology.

4 Attempt any **two** parts of the following : **10×2=20**

- (a) Explain various multiprocessor scheduling strategies in detail.
- (b) (i) Draw a data flow graph for following code block using $*$, $+$, $-$ and $/$ as arithmetic operators :

$x \leftarrow a + b;$

$y \leftarrow a * c;$

$z \leftarrow x + d;$

$x \leftarrow y - d;$

$x \leftarrow x + c;$

where a , b , c and d are constants.



- (ii) Indicate the events that can be done in parallel in the execution of the above block of code.
- (c) (i) Differentiate between Static data flow computer organization and Dynamic data flow computer organization.
- (ii) How does the data flow program mechanism differs from control flow mechanism.

Attempt any **four** parts of the following :

5×4=20

- (a) What is the difference between software interrupts and hardware interruptus ? Explain the functioning of RST instructions in 8085.
 - (b) Write a program in 8085 assembly language to add two 2-digit (8-bit) BCD numbers available at 2000 H, 2001 H memory locations.
 - (c) Define program status word. Which type of instructions affect the flag register ? Explain the role of Auxiliary carry flag in 8085.
 - (d) Explain the functions of HOLD and HLDA signals of the 8085 microprocessor.
 - (e) (i) Give example of one-byte, two-bytes and three-bytes instruction of 8085 microprocessor.
 - (ii) What is the advantage of using assembly language instead of writing a program directly in machine language.
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M. C. A.

(SEM. II) EXAMINATION, 2006-07
COMPUTER ARCHITECTURE &
MICROPROCESSOR

Time : 3 Hours

[Total Marks : 100

- Note :*
- (1) Attempt all questions.*
 - (2) All questions carry equal marks.*

1 Attempt any **two** parts of the following :

- (a) Explain four possible hardware schemes that can be used in an instruction pipeline in order to minimize the performance degradation caused by instruction branching.
- (b)
 - (i) Determine the number of pipe clock cycles that it takes to process 200 tasks in a six-segment pipeline.
 - (ii) A nonpipeline system takes 50 ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10 ns. Determine the speed up ratio of the pipeline for 100 tasks.
- (c) Explain the following :
 - (i) Serial versus parallel processing
 - (ii) Parallelism versus pipelining.

2 Attempt any **two** parts of the following:

- (a) Explain two techniques for enhancing the performance of computers with multiple execution pipeline.
- (b) The following overlaid reservation table corresponds to a two-function (A,B) pipeline.

	t_0	t_1	t_2	t_3	t_4
S_1	A	B		A	B
S_2		A		B	A
S_3	B		AB		

- (i) List all four cross forbidden lists of latencies and corresponding combined cross-collision matrices.
- (ii) Draw the state diagram for the two functional pipeline.
- (c) Suppose that scalar operations take 10 times longer to execute per result than vector operations. Given a program which is originally written in scalar code:
- (i) What are the percentage of the code needed to be vectorized in order to achieve the speed up factors of 2,4 and 6 respectively ?
- (ii) Suppose the program contains 15% of code that cannot be vectorized such as sequential I/O operations. Now repeat part (i) for the remaining code to achieve the three speed up factors.

3 Attempt any **two** parts of the following :

- (a) In case of SIMD inter connection networks, explain the various static interconnection network topologies.
- (b) Write down an $O(n^2)$ algorithm and an $O(n \log_2 n)$ algorithm for matrix multiplication and explain it.

- (c) Prove or disprove that the Omega network can perform any shift permutation in one pass. The shift permutation is defined as follows: given $N=2^n$ inputs, a shift permutation is either a circular left shift or a circular right shift of k positions, where $0 \leq k < N$.

4 Attempt any **two** parts of the following:

- (a) Explain the functional structures of Loosely coupled Microprocessors and Tightly coupled Microprocessors.
- (b) Explain the following:
- (i) List scheduling algorithm
 - (ii) Coffman and Graham algorithm.
- (c) (i) What are the major design issues towards the practical realization of a data flow computer ?
- (ii) What are the data flow graphs? Explain with the help of an example.

5 Attempt any **four** of the following :

- (a) What are tri-state devices and why are they essential in a bus-oriented system?
- (b) List three improved features of the 8085 over the 8080A microprocessor.
- (c) Define: Instruction cycle, machine cycle and T-state.
- (d) Write a program to :
- (i) Clear the accumulator
 - (ii) Add 47H (use ADI instruction)
 - (iii) Subtract-92H
 - (iv) Add 64H

- (v) Display the result after subtracting 92H and after adding 64H.

Specify the answers you would expect at the output ports.

- (e) Add the following five data bytes stored in memory locations starting 2060H and display the sum (the sum if less than FF. Use register B to store the partial sum). Write the program without using ADD M.
- (f) Write a 20 ms time delay subroutine using register pair BC. Clear the Z flag without affecting any other flags in the flag register, and returns to the main program.
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