Printed Pages : 7 **MCA – 215**

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 7307 Roll No. | | | | | | | | | | |

M. C. A.

(SEM. II) EXAMINATION, 2008-09

COMPUTER ORGANIZATION

Time : 3 Hours] *[Total Marks : 100*

Note : This paper is in **three** sections. Section A carries **20** marks, Section B carries **30** marks and Section C carries **50** marks.

SECTION–A

1 You are required to answer all the parts : **2×10=20**

Choose correct answer for the following parts :

(a) Exponent in floating point number representation is biased to :

(i) enhance the range of representation

(ii) avoid comparing sign bits of exponent in floating point arithmetic operation.

(iii) to facilitate representation of zeros

(iv) both (ii) and (iii) are true.

(b) A stack pointer register is always associated with a :

(i) hardwired stack

(ii) Software stack to indicate top of the stack element

(iii) Hardware stack to store stack capacity

(iv) None of the above is true.

(c) The implied one-bit to the left of fractional mantina of IEEE 754 floating point format is used to facilitate.

(i) enhancement of precision

(ii) representation of NaN (not a number) representation

(iii) enhancement of the range of representation;

(iv) representation of sign bit.

(d) Program size is likely to be minimum with :

(i) Expanding opcode

(ii) fixed length opcode

(iii) data dependent opcode

(iv) None of the statements is valid.

(e) A microprogram sequencer :

(i) enables efficient handling of microprogram subroutines.

(ii) help appropriate encoding and decoding of control signals in control memory.

(iii) control the generation of effective address for the control ROM.

(iv) handles the task of next address generation in a microprogrammed control structure.

(f) A typical vertical microinstruction format is characterized by :

(i) limited encoding with limited parallilism

(ii) limited encoding with high degree of parallilism

(iii) high degree of encoding with high degree of parallilism

(iv) high degree of encoding with limited parallilism.

(g) A CPU handles interrupt by executing interrupt service routine.

(i) whenever an interrupt is registered

(ii) by checking interrupt register after execution of each instruction.

(iii) by checking interrupt register at the end of fetch cycle.

(iv) by checking interrupt register at regular times interval.

(h) The CPU state is saved in the event of a transfer control.

(i) from one instruction to a non-sequential instruction of a program

(ii) from our program to another

(iii) during execution of an instruction due to an interrupt cycle.

(iv) None of the above statement is true.

(i) An instruction with an indexed operand having address field with all O's bit is effectively a'.

(i) register direct mode of operation

(ii) register indirect mode of operation

(iii) memory indirect mode of operation

(iv) base register addressing mode of operation.

(j) The delay element method of controller design employs:

(i) encoded control states

(ii) modulo-K counter to control K repetitive actions.

(iii) Control structure directly reflecting the behaviour

(iv) None of the above is valid.

SECTION–B

2 Answer any **three** parts of the following : **10×3=30**

(a) (i) Show the block diagram of the hardware that implements the following register transfer statement

$T : R2 \leftarrow R1, R1 \leftarrow R2$

(ii) Describe the design of 4-bit carrylook ahead adder.

(b) Write short notes on microprogram sequencing and microinstruction with next address field.

(c) Write a program to evaluate the arithmetic statement:

X = (A-B+C*(D*E-F)/(G+H*K) using three, two, one and zero address instructions.

(d) With the help of block diagram, discuss working of direct memory access (DMA). Also explain features of an IOP. Give a brief comparison of DMA and IOP.

(e) A block set associative cache consists of a total of 64 blocks divided into 4 block sets. The main memory contains 4096 blocks, each consisting of 128 words.

(i) How many bits are there in a main memory address?

(ii) How many bits are there in each of the TAG, SET and Word fields?

SECTION–C

3 Answer any **two** parts of the following : **5×2=10**

(a) Design an arithmetic circuit with one selection variable S and two n-bit data inputs A and B. The circuit generates the following four arithmetic operations in conjunction with the input carry C_{in}. Draw the logic diagram for the first two stages.

S	$C_{in}=0$	$C_{in}=1$
0	$D=A+B$(add)	$D=A+1$(increment)
1	$D=A-1$ (decrement)	$D=A+\overline{B}+1$(subtract)

(b) Design a digital circuit that performs the four logic operations of exclusive OR, exclusive - NOR, NOR and NAND. Use two selection variables. Show the logic diagram for the first two stages.

(c) What are the basic differences between a branch instruction, a call subroutine instruction and program interrupt?

4 Answer any **one** part of the following : **10×1=10**

(a) Explain the differences between hardwired control and microprogrammed control. What are advantages and disadvantages of hardwired and microprogrammed control?

(b) (i) Give the different characteristics of the RISC and CISC computers.

(ii) Explain micro-instruction format. Describe horizontal and vertical micro-instructions.

5 Answer any **two** parts of the following : **5×2=10**

(a) Describe the design of 4-bit carry look ahead adder.

(b) Define the following terms :

(i) Microoperation

(ii) Micro introduction

(iii) Microprogram

(iv) Microcode

(c) Represent following decimal numbers in IEEE 754 floating point format:

$\pm$ 1.75, $\pm$ 21

6 Answer any **one** part of the following : **10×1=10**

(a) Design a variable length opcode to allow all of the following to be encoded in a 36-bit instruction.

(i) Instruction with two 15-bit addresses and one 3-bit register number.

(ii) Instruction with one 15-bit address one 3-bit regtister number.

(iii) Instruction with no addresses or rigisters.

(b) A virtual memory system has 16 k word logical address space, 8k word physical address space with a page size of 2k words. The page address trace of a program has been found to be :

7 5 3 2 1 0 4 1 6 7 4 2 0 1 3 5

Note the four pages residents in memory after each page reference change for each of the following replacement policies :

(i) FIFO

(ii) LRU.

7 Answer any **two** parts of the folowing : **5×2=10**

(a) Show the step-by-step multiplication process using booth algorithm when the binary numbers (+15) * (-13) are multiplied. Assume 5-bit registers that hold signed numbers.

(b) Give atleast six status conditions for the setting of individual bits in the status register of an asynchronous communication interface.

(c) Write short notes on $2^{1/2}$ D memory organization.
