PAPER ID-311679

Subject Code: KCA105

Roll No: | | | | | | | | | | | | | |

MCA

(SEM I) THEORY EXAMINATION 2024-25

COMPUTER ORGANIZATION & ARCHITECTURE

TIME: 3 HRS **M.MARKS: 100**

Note: Attempt all Sections. In case of any missing data; choose suitably.

SECTION A

1. Attempt *all* questions in brief. **2 x 10 = 20**

Q no.	Question	CO	Level
a.	Compare the various addressing modes used in processor organization.	1	K2, K3
b.	How does bus width affect data transfer rates?	1	K2, K3
c.	Analyze the process of floating-point division and describe the challenges involved in implementing floating-point arithmetic in hardware.	2	K2, K4
d.	Explain the architecture of an ALU.	2	K2, K4
e.	Apply the principles of instruction pipelining and identify hazards that can occur in a pipeline.	3	K3
f.	Apply the concept of micro-operations in program control. Explain how control signals govern their execution.	3	K3
g.	Explain the trade-offs between speed, cost, and capacity.	4	K2, K3
h.	Analyze the impact of cache memory on processor performance.	4	K2, K3
i.	Explain Direct Memory Access.	5	K1, K2
j.	Explain synchronous and asynchronous serial communication.	5	K1, K2

SECTION B

2. Attempt any *three* of the following: **10 x 3 = 30**

Q no.	Question	CO	Level
a.	Explain the role of functional units. How do these units interact using system buses, and what are the different types of bus architectures used in modern computers?	1	K2, K3
b.	Explain how floating-point numbers are represented, normalized, and rounded, and discuss the implications of precision errors in scientific computations.	2	K2, K4
c.	Apply the concept of Reduced Instruction Set Computer and Complex Instruction Set Computer. Compare their architectural differences and analyze their impact on performance and power consumption.	3	K3
d.	Explain the design and performance considerations of cache memory. How do replacement policies affect cache performance?	4	K2, K3
e.	Analyze standard communication interfaces. How do these interfaces impact data transfer speed and system performance?	5	K1, K2

SECTION C

3. Attempt any *one* part of the following: **10 x 1 = 10**

Q no.	Question	CO	Level
a.	Understand the concept of bus arbitration and compare different bus arbitration techniques. How do these techniques impact system performance in multiprocessor environments?	1	K2, K3

Roll No: | | | | | | | | | | | | | |

MCA
(SEM I) THEORY EXAMINATION 2024-25
COMPUTER ORGANIZATION & ARCHITECTURE

TIME: 3 HRS **M.MARKS: 100**

b.	Remember the different types of registers in a processor and explain their specific functions. How does the use of general-purpose and special-purpose registers improve computational efficiency?	1	K2, K3

4. Attempt any *one* part of the following: 10 x 1 = 10

Q no.	Question	CO	Level
a.	Explain the concept of look-ahead carry adders and analyze how they improve addition speed compared to ripple carry adders. Explain their working principle with an example.	2	K2, K4
b.	Analyze Booth's algorithm for signed operand multiplication. Provide a step-by-step example of multiplying two signed binary numbers using Booth's algorithm and explain how it optimizes the multiplication process.	2	K2, K4

5. Attempt any *one* part of the following: 10 x 1 = 10

Q no.	Question	CO	Level
a.	Apply the concept of instruction cycles and sub-cycles to explain the complete execution of an instruction in a processor. How does instruction pipelining improve the efficiency of execution? Provide a detailed example.	3	K3
b.	Apply the differences between hardwired and microprogrammed control units. Design a simple microprogrammed control unit and explain how microinstructions are sequenced and executed.	3	K3

6. Attempt any *one* part of the following: 10 x 1 = 10

Q no.	Question	CO	Level
a.	Make use of the concept of virtual memory and explain how it is implemented using paging and segmentation. Discuss the role of the Memory Management Unit in address translation.	4	K2, K3
b.	Compare and contrast the differences between various types of secondary and auxiliary storage devices. How do advancements in storage technology impact computing performance?	4	K2, K3

7. Attempt any *one* part of the following: 10 x 1 = 10

Q no.	Question	CO	Level
a.	Explain the different types of I/O interfaces and their role in computer architecture. Explain how memory-mapped I/O differs from isolated I/O and discuss their advantages and disadvantages.	5	K1, K2
b.	Analyze the different types of interrupts and their role in handling external and internal events in a computer system. How does interrupt priority affect system performance?	5	K1, K2