Printed Pages : 4

NMCA-115

(Following Paper ID and Roll No. to be filled in your Answer Book)

PAPER ID : 214121

Roll No.

M. C. A.

(SEM. I) (ODD SEM.) THEORY EXAMINATION, 2014-15

DIGITAL LOGIC DESIGN

Time : **3** Hours] [Total Marks : **100**

Note : Attempt all questions. Each question carries equal marks.

1 Attempt any **four** parts of the following : **(5×4=20)**

a) Perform the following arithmetic operations

i) Add $(-38)_{10}$ and $(56)_{10}$ using 2's complement method

ii) Add $(43)_{10}$ and $(-72)_{10}$ using 1's complement method.

b) What are error detecting and correcting codes ? The 7 bit hamming code 1011101 is received at the receiving end. Correct the received data if there is any error. There are four parity bits and even parity is used.

c) What is 32 bit IEEE 754 floating point representation ? Represent 412.625 in single floating point representation.

d) Obtain the minimised SOP expression for the function $F(a,b,c,d) = \sum m(2,3,5,7,9,13,14,15) + \sum dc(10,11,12)$. Here m denotes the minterm and dc denotes the don't cares.

e) Give NOR implementation of AND, OR and NOT gates. Convert $(772)_8$ in equivalent decimal and hexadecimal code.

f) Minimize the following Boolean function using tabular method (Quine Mc-Clusky method).Find the prime implicants and essential prime implicants.

$F(A,B,C,D) = \sum m(0,1,5,7,8,10,14,15)$

2 Attempt any **four** parts of the following : **(5×4=20)**

a) Draw and explain the working of full adder using two half adders.

b) For the Boolean function

$F(w,x,y,z) = xy'z + x'y'z + w'xy + wx'y + wxy$

i) Obtain the truth table of F

ii) Draw the logic diagram using the original Boolean expression.

iii) Use the Boolean algebra to simplify the function to a minimum number of literals.

iv) Obtain the truth table of the function from the simplified expression and show that it is the same as the one in part (i).

c) Implement the following Boolean function using 8:1 multiplexer:

$F(W,X,Y,Z) = \sum m(0,1,2,3,4,10,11,14,15)$

d) Draw the combinational circuit and briefly explain the functioning of BCD Adder.

e) What is a binary multiplier ? Draw and explain the working of 2 × 4 decoder.

f) Draw the magnitude comparator that compares 3 bits of data and explain its working.

3 Attempt any **two** parts of the following : **(10×2=20)**

a) What is the shift register ? Draw and explain the working of 4 bit universal shift registers.

b) What is the difference between synchronous and asynchronous sequential circuit ? Describe the state reduction technique and the state assignment technique in synchronous sequential circuit.

c) Design a BCD synchronous counter using T Flip Flop. Check whether the counter is self starting or not. If not use the 'Reset' signal to make it self starting.

4 Attempt any **two** parts of the following : **(10×2=20)**

a) Write short notes on the following :

i) Comparison between PLA , PAL and PROM

ii) Structure and working of 4 × 4 RAM

b) Draw the (i) ASM chart (ii) state diagram (iii) state table for a 2-bit up down counter having mode control input.
M=1: Up Counting M=0: Down Counting
Design the circuit using multiplexer.

c) Difference between ASM and Flow Charts. Implement and tabulate the PAL programming table for the full adder.

5 Attempt any **two** parts of the following : **(10×2=20)**

a) An asynchronous sequential circuit is described by the excitation function

$$Y = x_1' x_2' + \left(x_1' + x_2\right) y$$

and the output function
Z = Y

i) Draw the logic diagram of the circuit.

ii) Derive the transition table and output map.

iii) Obtain a two state flow table.

iv) Describe in words the behaviour of the circuit

b) What are hazards ? Explain hazards in combinational and sequential circuit. Explain the static 0, static 1 and dynamic hazard. Explain some way of eliminating hazards. What are critical and non critical race.

c) Write short notes on the following :

i) Comparison of latches with flip flops

ii) Block diagram and working of asynchronous sequential circuits

iii) Steps for design of asynchronous sequential circuits

iv) Merger graph and implication table with example.
