

(Following Paper ID and Roll No. to be filled in your Answer Book)

Paper ID : 214105

Roll No.

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MCA

(SEM. I) THEORY EXAMINATION, 2015-16

DIGITAL LOGIC DESIGN

[Time:3 hours]

[Total Marks:100]

Note : Attempt questions from all Sections as per directions.

Section-A

1. Attempt **all** parts. Write answer of each part in brief.

(10x2=20)

- (a) The solutions to the quadratic equation $x^2-11x+22=0$ are $x=3$ and $x=6$. What is the base of the numbers.
- (b) List all the minterms for three variable x , y , and z ?
- (c) Define multiplexer? Draw a logic diagram of 4×1 multiplexer.
- (d) Write the truth- table of an octal-to binary priority encoder.

- (e) Explain the race condition in the context of SR flip-flop?
- (f) Show that the characteristic equation for the complement output of JK flip-flop is $Q'(T+1) = J'Q' + KQ$.
- (g) Explain the difference between EPROM and EEPROM.
- (h) How many address line and input-output data lines are required for memory unit $8K \times 8$?
- (i) Discuss how ASM chart differs from conventional flow chart?
- (j) Define critical race and non-critical race.

Section-B

Attempt any five questions from this section. (10x5=50)

2. (a) Perform the following conversions as directed:
- (i) $(64CD)_{16} \rightarrow (?)_8$ (1X5)
 - (ii) $(DADA.B)_{16} \rightarrow (?)_{10}$
 - (iii) $(10110.0101)_2 \rightarrow (?)_{10}$
 - (iv) $(268.75)_{16} \rightarrow (?)_8$
 - (v) $(867)_{16} \rightarrow (?)_{BCD}$

(b) Do as directed:

$$\left(2\frac{1}{2}\times 2\right)$$

(i) Represent $(-89)_{10}$ in 2's complement representation using 8-bits.

(ii) Find the decimal equivalent of binary $(10111011)_2$. Assume the given number in 1's complement representation.

3. (a) Simplify the Boolean function f together with don't care condition d in SOP and POS:

$$f(w,x,y,z) = \sum (0,1,2,3,7,8,9,10)$$

$$d(w,x,y,z) = \sum (5,6,11,15)$$

(b) Define binary adder. Draw the logic circuit of a 4-bit binary adder-subtractor and explain its working.

4. A majority circuit is a combinational circuit whose output is equal to 1 if the input variables have more 1's than 0's. The output is 0 otherwise. Design a 3-input majority circuit by finding the circuit's truth-table, Boolean equation, and a logic diagram.

5. list the capabilities of general shift register? Draw the logic circuit of "4-bit bidirectional shift register with parallel load" and explain its working?

6. Design a 2 bit count-down counter. When input $x=0$, the state of the flip-flop does not change. When $x=1$, the state sequence is 11,10,01,00,11 and repeat. Draw the state diagram.
7. (a) Draw a PLA circuit to implement the functions
- $$F_1 = A'B + AC' + A'BC'$$
- $$F_2 = (AB + AC + BC)'$$
- (b) Explain decision box and conditional box used in ASM chart.
8. (a) Derive the ROM programming table for the combinational circuit that squares a 4-bit number. Minimize the number of product terms.
9. (a) Draw the logic configuration of four inputs and four outputs PAL and explain it.
- (b) Discuss different types of hazards in combinational and sequential circuits.

Section-C

Attempt any two questions from this section. (15x2=30)

10. (a) Find all the prime implicants for the following boolean functions, and determine which are the essential prime implicants. (5)

$$f(w,x,y,z) = \sum (0,2,4,5,6,7,8,10,13,15)$$

- (b) Implement full- subtrator circuit using multiplexer of suitable size. (5)
- (c) Design a Binary multiplier circuit that multiplies two binary numbers, where first number is of 4-bits and second number is of 3 bits. Use AND gates and binary address. (5)
11. (a) A PN flip-flop has four operation: clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10 and 11, respectively. (2×4)
- Tabulate the characteristic table.
 - Derive the characteristic equation.
 - Tabulate the excitation table.
 - Show how the PN flip-flop can be converted to a D flip-flop.
- (b) The following is a truth table of a three-input, four-output combinational circuit:

Inputs			Outputs			
x	y	z	A	B	C	D
0	0	0	0	1	0	0
0	0	1	1	1	1	1
0	1	0	1	0	1	1
0	1	1	0	1	0	1
1	0	0	1	1	1	0
1	0	1	0	0	0	1
1	1	0	1	0	1	0
1	1	1	0	1	1	1

Tabulate the PAL programming table for the circuit, and mark the fuse map in a PAL diagram. (7)

12. (a) Draw the block diagram of asynchronous sequential circuit and explain its working. (5)
- (b) An asynchronous sequential circuit has two internal states and one output. The excitation functions and output function of the circuit are as follows:

$$Y_1 = a'b + bx$$

$$Y_2 = ay + x$$

Output function

$$Z = a + y$$

- (i) Derive the logic diagram of the circuit. (5)
- (ii) Derive the transition table and output map. (5)

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