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Sub Code: RCA104

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Roll No. | | | | | | | | | | |

MCA
(SEM I) THEORY EXAMINATION 2017-18
COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 3 Hours

Total Marks: 70

Note: 1. Attempt all Sections. If require any missing data; then choose suitably.
2. Any special paper specific instruction.

SECTION A

1. **Attempt *all* questions in brief.** 2 x 7 = 14
   a. Find 2's complement of $(11000100)_2$.
   b. What is micro instruction?
   c. What is Von Neumann bottleneck? How can this be reduced?
   d. what is cache updating? Why is it necessary?
   e. What is system bus? Explain different type of bus.
   f. What are characteristic of a good instruction format?
   g. Explain valid bit with example.

SECTION B

2. **Attempt any *three* of the following:** 7 x 3 = 21
   a. Explain the following.
      I. Bus structure
      II. Multiple bus hierarchy.
   b. What are the major functions of a processor? Explain them with the help of a flow chart.
   c. What are the parameters of a typical hierarchical memory system? Derive the average access time T formula of a n-level hierarchical system.
   d. Explain the working and action of DMA with the help of a suitable example.
   e. A computer has 32 bit instruction and 12 bit address. If there are 250 two-address instructions, how many one-address instructions can be formulated?

SECTION C

3. **Attempt any *one* part of the following:** 7 x 1 = 7
   a. Draw and explain the block diagram of a simple computer with 5 functional units.
   b. Explain various OS types in detail.

4. **Attempt any *one* part of the following:** 7 x 1 = 7
   a. What is the purpose of swapping? Explain the purpose of a translation look aside buffer in ARM memory management with block diagram.

b. Explain Booth's algorithms for 2's complement multiplication using flow chart. use the Booth algorithm to multiply 23(multiplicand) by 29(multiplier), where each number is represented using 6 bit.

5. **Attempt any *one* part of the following:** **7 x 1 = 7**

a. Discuss RISC & CISCs.

b. What is cache coherence? How can theproblems related to itbe resolved? Can this problem occur in uniprocessor system?

6. **Attempt any *one* part of the following:** **7 x 1 = 7**

a. Discuss Flynn's classification of various computer architecture with the help of their functional block diagram.

b. State Amdahl's Law. Show the derivation of speed ratio with variation of number of processors with reference to the fraction of series component in parallel computation.

7. **Attempt any *one* part of the following:** **7 x 1 = 7**

a. Write short note on following

I. Data manipulator

II. VLIW processor

b. Attempt the following

I. Explain Interlocks and Hazards.

II. Describe a parallel addition algorithm on a S/MD architecture.