



Supporting Document

1.1.1 The Institution ensures effective curriculum delivery through a wellplanned and documented process.

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	Internal Assessment	
	External Assessment	

IMS ENGINEERING COLLEGE, GHAZIABAD ACADEMIC CALENDAR (As per AKTU) (ODD SEM: 2020 - 21) [Version-1]

	Oct-20											
М	Т	T W T F		F	s							
			1	2	3	4						
5	6	7	8	9	10	11						
12	13	14	15	16	17	18						
19	20	21	22	23	24	25						
26	27	28	29	30	31							
		T/ W	Days :	19/21								

			Nov-20)		
М	Т	W	V T F		S	
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9	10	11	12	13	14	15
16	17	18	19	20	21	22
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30						
		T/ W Da	ays : (1	6+3)/20)	

	Dec-20											
М	F	W	Г	F	s							
	1	2	3	4	5	6						
7	8	9	10	11	12	13						
14	15	16	17	18	19	20						
21	22	23	24	25	26	27						
28	29	30	31									
	-	T/ W	Days :	17/24	-	-						

			Jan-21			
Μ	Т	W	Т	F	S	
				1	2	3
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25 26		27	28	29	30	31
		T/ W	Days :	15/22		

Feb-21											
Μ	Т	T W T F		S							
1	2	3	4	5	6	7					
8	9	10	11	12	13	14					
15	16	17	18	19	20	21					
22	23	24	25	26	27	28					
		T/ W	Days :	20/22							

			Mar-21											
Μ	Т	T W T F		F	S									
1	2	3	4	5	6	7								
8	9	10	11	12	13	14								
15	16	17	18	19	20	21								
22	23	24	25	26	27	28								
29 30		31												
		T/ W	Days :	5/23										

IMPORTANT DATES	HOLIDAYS	EXAMINATION / CLASS TEST				
Commencement of Classes for 2nd, 3rd & 4th Yr: 5 th Aug	14, 15 & 16 NOV (SAT, SUN & MON): Deepawali	CT-1 : 2 nd -DEC to 8 ^{th-} DEC, 2020				
Commencement of Classes for 1st & 2nd (Lateral) 25 th NOV	30-NOV (MON) : Guru Nanak's B'day	CT-2 : 19, 21, 26, 28-DEC, 2, 4 JAN 2021				
	25-DEC (FRI) : Christmas Day	PUT : 18 th JAN to 23 rd JAN, 2021				
	11-MAR (THU) : Maha Shivratri	(3 rd & 4 th Year AKTU External)				
Upload Assignment (Important Dates)	28-MAR (SUN) : Holika Dahen	AKTU End Sem Exam (01-FEB to 20-FEB, 2021)				
	29-MAR (MON) : Holi	(1 st & 2 nd Year AKTU External)				
		AKTU End Sem Exam (08-MAR to 20-MAR, 2021)				
		AKTU End Sem Practical Examination				

Total Teaching Days/Working Days (T/W): 60/132 [95/132]

Faculty members are requested to 1) Upload the attendance after completion of the class (L/T/P) itself on the same day. 2) Upload / Check / Submit the assignment as per schedule (weekly).

Advance digited system using verifieres &. REC-401 minin 6 miniscuntul	Subject: NEC 02 4P		Hand	Wr B Galat Sardan - 2. John H. Davies	J. NO. Author	Respected Sir It is recommended the	To The Director Sir IMSECS, Ghaziabad
design John Raun	Teacher Into a		basics Litedition	MSPH30 Microcontroller	· Design through they los	at the following books may be purcha	S
CLE Keymonon Keymonon Dean (Academics)			Publication 102	Publication 200	Publication Copies Reqd.	sed for the college library	CENTRAL LIBRARY OKS REQUISITION FORM
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Director Sin			525/- 53 Per c+y 53	its (22.17) setting	ppies Appx. Price Amt	ester:	/1/11 (2017- LECH/MBA/MCA/M.Tech)
			550/- 4th	49 000	. (INR)		18

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202 41 0 30 S.No. Author 50 03 Competer × 5035 Sig Boten Sound remained Subject: The Director Sir It is recommended that the following books may be purchased for the college library. Sanction for purchase may please be accorded. To Respected Sir IMSECS, Ghazlabad HYOUM TUY bach Achange Setu, Ullwan Aso, Laun ger Fressmen Sig Data Analytics Knewledge based Jecilian regarson Sattware Engineering Compiler Degin 1 tightal & Ama Communication Syleuns A N 2. For 5 or Ringian 2. For supplies Insur First inperation most the Teacher (s): FEINS IMS L. FREERING COLLEGE, GHAZIABAD BOOKS REQUISITION FORM will ey CENTRAL LIBRARY Reauson Willey Publication HSH Deen & Academica And PLC . Brut . Copies Reqd. No. of Students Existing copies 4500 10 2 20.12.16. 110 0 2 102 0 5 91 3 rear/semester: 122 yr (xith Seu) Course: (B.Tech/MBA/MCA/M.Tech) Branch: 1T Date: 15/14/2016 (2016-17) XIL XIL 30 24 91 1668 Appx. Price Amt (INR) 1/882 619/ 625 497 Director Sir 15/12/6 9 prairie upole Sh al

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3 12 -1 E S.No. 5 -3 + 69 10 . 0.5 IMSECS, Ghaziabad The Director Sir . To It is recommended that the following books may be purchased for the college library. Sanction for purchase may please be accorded. Respected Sir subject: Author Galynn SN Decho シャナト Tay Yauthan Multimedia: Making S N SNYADAN Toc Sam P Putt + 200 C Proceso Human Values & Profer Ethics Theory of Computer Science: PHI Communication System tutomate, Lary. 4 Computation Industrial Socialogy Operating Systems Concepts Wiley angitat & Analo The principles of soft computing where CONTRACTION STREWLL (2nd edition) 17 work Teacher (s): 3 HOD AND Dean (Academical MIL BOOKS REQUISITION FORM CENTRAL LIBRARY Endia HWL Whiley John Publication NIL 0 Kap : Copies Reqd. No. of Students Existing copies Appx Price Rep とこし Aug : 42 - Mart 10,60 1-1-1 1-12 NIL -00 1-00 22 Cofer & Ked 52 92 0 57 LON 60 92 r r Manne. Branch: I T Course: (B.Tech/MBAMMCATT Tech) Year/Semester: 4th Europeter Date: 92 50 92 22 LI 60 el Ma mercare Intales ferra 275 623 SIS 629 **Director Sir** D Ray P 2015-15) Amt. (INR) 31100 0556 11520 20128 Con . DE P. (D)

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Subject: Interpreted Circuid Tech			/	1. SM. SZE	S.No. Author	To The Director Sir IMSECS, Ghaziabad Respected Sir It is recommended th
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IMS ENGINEERING COLLEGE, GHAZIABAD DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING CACUL TY LOAD EVEN SEMESTER (SESSION 2019-20)

	r:	Subject	LOAD EVEN SEMIESTER (SEE	Uni	v. L	oad	Tata	Act	ual L	oad	Total
SI.	Faculty Name	Code	Subject	L	Т	Р	Total	L	Т	Р	Total
	Prof. (Dr.) R. P. S.	KCS403	Microprocessor (CS1)	3	1	0	8	4	2	0	12
1	Chauhan (HOD)	KCS403	Microprocessor (CS2)	3	1	0		4	2	0	
		REC 085	Wireless & Mobile Communication (EC1)	3	1	0		4	2	0	
2	Prof. (Dr.) R. N. Baral	REC 085	Wireless & Mobile Communication (EC2)	3	1	0	12	4	2	0	16
		REC 651	Microwave Engineering Lab (EC2)	0	0	4		0	0	4	
	Prof. Pankaj Goel	REC 064	Advance Digital Design Using Verilog (EC1)	3	1	0	8	4	2	0	12
3	(Dean, DSW)	REC 064	Advance Digital Design Using Verilog (EC2)	3	1	0	0	4	2	0	
		KEC 401	Communication Engineering	3	0	0		5	0	0	
4	Prof. (Dr.) Ram Sewak Singh	KEC 451	Communication Engineering Lab	0	0	4	11	0	0	4	15
	, a	REC 080	Electronics Switching (EC1)	3	1	0		4	2	0	
_	D.(D.	KEC 402	Analog Circuit	3	1	0		4	2	0	
	Kumar	KEC 452	Analog circuit Lab	0	0	4	11	0	0	4	15
		RIC 603	Control System I (EC2)	3	0	0		5	0	0	
	D- EL N	KOE 048	Electronics Engineering (CS1)	3	1	0		4	2	0	
6	Vashishtha	KOE 048	Electronics Engineering (CS2)	3	1	0	12	4	2	0	16
		RIC 651	Microcontrollers for Embeded System Lab (EC2)	0	0	4		0	0	4	
	Prof Proven	REC 601	Microwave Engineering (EC1)	3	1	0		4	2	0	
7	Chaurasia	REC 601	Microwave Engineering (EC2)	3	1	0	12	4	2	0	16
1	and the second second	RIC 651	Microcontrollers for Embeded System Lab (EC1)	0	0	4		10	0	4	
		REC 602	Digital Communication (EC1)	3	0	0		5	0	0	
8	Prof. Balwant	REC 602	Digital Communication (EC2)	3	0	0		5	0	0	
	Singh	REC 652	Communication Lab II (EC1)	0	0	4	14	0	0	4	18
		REC 652	Communication Lab II (EC2)	0	0	4		0	0	4	
		ROE082	Entrepreneurship Development (EC1)	3	0	0		5	0	0	
9	Prof. Ravi Kumar	ROE082	Entrepreneurship Development (EC2)	3	0	0	10	5	0	0	14
)		RIC 653	Control System lab I (EC2)	0	0	4		0	0		14
	Prof. (Dr.) Neerai	KEC 403	Signal System	3	1	0		4	2	*	
10	Jain	KEC 453	Signal System Lab	0	0	4	12	1		0	
		REC 080	Electronics Switching (EC1)	3	1	0		4	0	4	16
		KOE 048	Electronics Engineering (CS3)	3	1			4	2	0	
11	Prof. V. K. Agrawal	KOE 048	Electronics Engineering (CS4)	3	1	0		4	2	0	
		KCS453	Microprocessor Lab (CS3)	0	1	-	16	4	2	0	20
	Prof Manual	KCS453	Microprocessor Lab (CS4)		0	4		0	0	4	
12	Saxena	KOE044	Sensor and Instrumentation	2		4		0	0	4	
12		RIC 653	Control System lab I (EC1)	3	1	0		4	2	0	
_		RIC 603	Control System I (EC1)		0	4	12	0	0	4	16
13	Prof. Arjun Singh	REC065	RADAR Engineering (EC1)	3	1	0		4	2	0	
10	Katiyar	REC065	RADAR Engineering (EC2)	3	1	0		4	2	0	
		REC 651	Microwave Engineering Lab (Ec.1)	3	1	0	12	4	2	0	16
				0	0	4		0	0	4	1
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HoD, ECE

IMS ENGINEERING COLLEGE, GHAZIABAD DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

FACULTY LOAD ODD SEMESTER (SESSION 2018-19)

			NAMES OF A DESCRIPTION OF A DESCRIPTIONO	2 J							
SL.	Faculty Name	Subject	Subject	Uni	versit	Load	Total	Ac	tual I	Load	Total
_		Code		L	T	P	1.575.41	L	T	P	Total
1	Prof. Rahul Dayal	REC-051	Antenna and Wave Propagation (EC1) *	3	1	0	. 8	4	0	0	9
_	· · · · · · · · · · · · · · · · · · ·	REC-051	Antenna and Wave Propagation (EC2) *	3	1	0	0	4	0	0	0
		ROE-033	Laser Systems and Application (ME1)	3	1	0		4	0	0	
2	Prof. Manish Zadoo	ROE-033	Laser Systems and Application (ME2)	3	1	0	1	4	0	0	1.
		RAS-501	Managerial Economics (CS3)	3	. 0	0	1.4	3	0	0	1 14
		RAS-501	Managerial Economics (2CS)	3	0	0		3	0	0	1
		REC-301	Digital Logic Design (EC2)	3	0	0		4	0	0	1
3	Prof. R. N. Baral	NOE-072	Quality Management (EC1)-4th Yr	3	0	0	9	5	0	0	14
		NOE-072	Quality Management (2EC)-4th Yr	3	0	0		5	0	0	1
		NEC-703	VLSI Design (EC1)	3	1	0		5	0	0	
4	Prof Pankai Cost	NEC-703	VLSI Design (EC2)	3	1	0		5	0	0	1
*	eren cantral over	REC-354	Electronics Workshop & PCB Lab (EC1 + EC2)	0	0	4	14	0	0	8	20
		RAS-302	Environment & Ecology (EC1)	2	0	0		2	0	0	
		REC-303	Signals & Systems (EC1)	3	1	0		4	4	0	
5	Prof. Abhishek Sharma	REC-303	Signals & Systems (EC2)	2	1	0	12	4	1	0	24
		REC-353	Signals & Systems Lab (EC1) + (EC2)	0	1		12	4	4	0	24
		NEC-703	VLSI Design (2EC)	2	1	4		0	0	8	_
2		RAS-501	Managerial Economics (EC1)	2	1	0		5	0	0	
6	Prof. Neeraj Jain	RAS-501	Managerial Economics (EC1)	2	0	0		3	0	0	
		NEC-752A	Electronics Circuit Design Lab (EC1 B1 + EC2 B1)	3	0	0	14	3	0	0	19
		NEC-752A	Electronics Circuit Design Lab (ECT B1 + ECZ B1)	0	0	2		0	0	4	
		REC 501	Integrated Circuits (EC2)	0	0	2		0	0	4	
		REC-501	Integrated Circuits (EC2)	3	1	0		4	4	0	
7	Prof. J. N. Vashishtha	DAS 302	Environment & Feelers (FC2)	3	1	0	12	4	4	0	22
		RA3-502 REC-551	Integrated Circuits Lab (EC1)	2	0	0		2	0	0	
		DEC 202	Floatnories Devices & Circle (ECI)	0	0	2		0	0	4	
•		REC-302	Electronics Devices & Circuits (ECI)	3	1	0		4	0	0	
0	Drof Drawoon Vumar	REC-302	Electronics Devices & Circuits (EC2)	3	1	0		4	0	0	
*	riot. riaveeli Kuillai	NEC-/52A	Electronics Circuit Design Lab (EC2 B2)	0	0	1	13	0	0	2	18
•		REC-352	Electronics Devices & Circuits Lab. (EC2)	0	0	2		0	0	4	
-		REC-352	Electronics Devices & Circuits Lab. (EC1)	0	0	2		0	0	4	
		REE-305	Network Analysis & Synthesis (EC1)	3	0	0		4	4	0	
9	Prof. Sujeet Kumar	REE-305	Network Analysis & Synthesis (EC2)	3	0	0	10	4	4	0	
		REC-552	Communication Lab - 1 (EC1)	0	0	2	10	0	0	4	24
_	and the second	REC-551	Integrated Circuits Lab (EC2)	0	0	2		0	0	4	
		NEC-032	Digital Image Processing (EC1)	3	1	0		5	0	0	
0	Prof. Praveen Chaurasia	NEC-032	Digital Image Processing (EC2)	3	1	0		5	0	0	
		RAS-501	Managerial Economics (CS1)	3	0	0	14	3	0	0	16
		RAS-501	Managerial Economics (CS2)	3	0	0		3	0	0	
		NEC-701	Optical Communication (EC1)	З	1	0		5	0	0	-
11	Prof. Ravi Kumar	NEC-032	Digital Image Processing (2EC)	3	1	0		5	0	0	
		NEC-751	Optical Communication & Networking Lab (EC1 B1)	0	0	1	13	0	0	2	20
_		REC-554	CAD of Electronics Lab-1 (EC1 + EC2)	0	0	4		0	0	2	
		REC-503	Digital Signal Processing (EC1)	3	1	0		4	-	0	
12	Prof Palmant Cinch	REC-503	Digital Signal Processing (EC2)	3	1	0		4	4	0	
	FIOL Balwant Singh	REC-553	Digital Signal Processing Lab. (EC1)	0	-	0	12	4	4	0	24
		REC-553	Digital Signal Processing Lab. (EC2)	0	0	-		0	0	4	
		REC-301	Digital Logic Design (CS1)	0	0	-2	-	0	0	4	
2	Dect to a feat of the	REC-301	Digital Logic Design (CS2)	3	0	0		5	0	0	
3	Prot. Jyoti Guglani	REC-351	Digital Logic Design Lab. (CS1)	3	0	0	10	5	0	0	18
		REC-351	Digital Logic Design Lab. (CS1)	0	0	2		0	0	4	10
1		NEC-701	Optical Communication (EC2)	0	0	2		0	0	4	
		NEC-701	Ontical Communication (BC2)	3	1	0		5	0	0	
4	Prof. Arjun Singh Katiyar	RECOSI	Antenna and Ways Brown (LEC)	3	1	0		5	0	0	
	and the second sec	NEC-751	Ordenta and wave Propagation (ECI) *	3	1	0	15	4	0	0	20
		NEC 441	Optical Comm. & Networking Lab (2EC1 B2)	0	0	1		0	0	2	
1		DEC. FOR	Optical Comm. & Networking Lab (EC1 B2 + EC2 B1)	0	0	2		0	0	4	
5	Prof. Arashdeen Vaur	DEC SUZ	Principles of Communication (EC1)	3	0	0		4	4	0	
1	eron maandoop naut	REA SHOT	Principles of Communication (EC2)	3	0	0	10	4	4	0	22
medi		MA3-302	Environment & Ecology (IT1 + IT2)	4	0	0		6	0	0	

1		NEC-702B	Data Communication Network (2EC)	3	1	0	T	5	0	10	-
		RAS-502	Sociology (EC1)	3	0	0	1	2	0	0	1000
16	Prof. Pooia Goel	RAS-502	Sociology (EC2)	3	0	0		2	0	0	
		NEC-752A	Electronics Circuit Design Lab (EC1 B2)	0	0	1	14	0	10	7	17
		NEC-751	Optical Communication & Networking Lab (EC2 B2)	0	0	1	1	1 a	0	2	
		REC-552	Communication Lab - 1 (EC2)	0	0	2		0	0	A	
		NEC-702B	Data Communication Networks (EC1)	3	1	0	-	5	0	0	-
17	Prof. Kamakehi	NEC-702B	Data Communication Networks (EC2)	3	1	0	1	5	0	0	
	a ron namarsin	REC-051	Antenna and Wave Propagation (EC2) *	3	1	0	14	A	0	0	16
		NEC-751	Optical Communication & Networking Lab (2FC B1)	0	0	2	1	10	0	2	
		REC-301	Digital Logic Design (CS3)	2	1	0	-	5	0	0	
18	Prof. V. K. Agarwal	REC-301	Digital Logic Design (2CS)	2	1	0		2	0	0	
	eren rene regar mar	REC-351	Digital Logic Design Lab (CS3)	0	1	2	12	10	0	-	18
-		REC-351	Digital Logic Design Lab. (2CS)	0	0	2	1	0	0	7	
		NOE-072	Quality Management (EC2)-4th Yr	3	0	0		5	0	3	-
14	Prof. Ram Sewak Singh	REC-301	Digital Logic Design (EC1)	3	0	0	10	4	0	0	17
-+		REC-351	Digital Logic Design Lab. (EC1 + EC2)	0	0	4		0	0	8	
		REC-301	Digital Logic Design (IT1)	3	0	0		4	2	0	
20	Prof. Mayurika Saxena	REC-301	Digital Logic Design (IT2)	3	0	0	1	4	2	0	
		REC-351	Digital Logic Design Lab. (IT1)	0	0	2	10	0	0	4	20
-		REC-351	Digital Logic Design Lab. (IT2)	0	0	2	1	0	0	4	
21	Prof. Pravesh Srivastava	RAS-301	Maths-III (EC1)	3	1	0		3	4	0	
_		RAS-301	Maths-III (EC2)	3	1	0	8	3	4	0	14

REC-051 Allocated to Prof. Arjun Singh and Prof. Kamakshi due to medical condition of Prof. Rahul Dayal.

1. Faculties Teaching in ECE Department: 16

- 2. Faculty Teaching in CSE Department: 2
- 3. Faculty Teaching in IT Department: 1
- 4. Faculty Teaching in ME Department: 1
- 5. Faculty Teaching from AS&H Department: 1

09-07-18

18.85

IMS ENGINEERING COLLEGE, GHAZIABAD DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING FACULTY LOAD EVEN SEMESTER (SESSION 2018-19)

1.	Faculty Name	Subject	Subject	live	rsit	y Lo	Total	Act	uall	load	Tota
+	Deef Dahul Daval	Lode	INITION PLAT MANA COMPANY (POAL)	L	T	P		L	T	P	
	Prof. Kanul Dayai	RAS 601	INDUSTRIAL MANAGEMENT (EC1)	3	0	0	6	3	0	0	6
+	(HOD)	RAS 601	INDUSTRIAL MANAGEMENT (EC2)	3	0	0		3	0	0	-
	Prof. Pankaj Goel	REC 405	INTRODUCTION TO MICROPROCESSOR (CSE DEPT)	3	0	0		5	0	0	
4	(Dean, DSW)	REC 405	INTRODUCTION TO MICROPROCESSOR (CSE DEPT)	3	0	0	8	5	0	0	14
+		RIC 651	MICROCONTROLLER AND EMBEDDED SYSTEM LAB	0	0	2		0	0	4	-
		NEC 801	WIRELESS & MOBILE COMMUNICATION	3	1	0		5	0	0	
3	Prof. R.N. Baral	RVE 401	UNIVERSAL HUMAN VALUES & PROFESSIONAL ETHICS	3	0	0	10	3	0	0	11
+		RVE 401	UNIVERSAL HUMAN VALUES & PROFESSIONAL ETHICS	3	0	0		3	0	0	-
		NEC 802	OPTICAL NETWORK	3	1	0		5	0	0	
4	Prof. Ram Sewak Singh	NEC 802	OPTICAL NETWORK	3	1	0	10	5	0	0	14
+		REC 453	ELCTRONIC MEASUREMENT & INSTRUMENTATIONS LAB	0	0	2		0	0	4	
		REC 602	DIGITAL COMMUNICATION	3	0	0		5	0	0	
5	Prof. Abhishek Sharma	NEC 802	OPTICAL NETWORK	3	1	0	9	5	0	0	14
		REC 652	COMMUNICATION LAB II	0	0	2		0	0	4	
		REC 401	MICROPROCESSOR & MICROCONTROLLERS	3	0	0		5	0	0	
5	Prof. Jyoti Guglani	REC 401	MICROPROCESSOR & MICROCONTROLLERS	3	0	0	8	5	0	0	14
		REC 451	MICROPROCESSOR & MICROCONTROLLERS LAB	0	0	2		0	0	4	
		RIC 603	CONTROL SYSTEM -1	3	0	0		5	0	0	
7	Prof. Praveen Kumar	NEC 044	ADVANCE DEGITAL DESIGN USING VHDL	3	1	0	9	5	0	0	14
		RIC 653	CONTROL SYSTEM LAB-1	0	0	2		0	0	4	
		ROE 041	INTRODUCTION TO SOFT COMPUTING	3	1	0		4	2	0	
8	Prof. J.N. Vashishtha	ROE 041	INTRODUCTION TO SOFT COMPUTING	3	1	0	10	4	2	0	16
		REC 452	ADVANCE ELECTRONIC SYSTEM LAB	0	0	2		0	0	4	
		REC 064	ADVANCE DIGITAL DESIGN USING VERILOG	3	1	0		4	2	0	
9	Prof. Sujeet Kumar	REC 064	ADVANCE DIGITAL DESIGN USING VERILOG	3	1	0	10	4	2	0	16
		REC 452	ADVANCE ELECTRONIC SYSTEM LAB	0	0	2		0	0	4	
1		REC 402	ELECTROMAGNETIC FIELD THEORY	3	1	0		4	2	0	
0	Prof. Praveen Chaurasia	REC 402	ELECTROMAGNETIC FIELD THEORY	3	1	0	10	4	2	0	16
		REC 451	MICROPROCESSOR & MICROCONTROLLERS LAB	0	0	2		0	0	4	
1		NEC 801	WIRELESS & MOBILE COMMUNICATION	3	1	0		5	0	0	
11	Prof. Balwant Singh	REC 602	DIGITAL COMMUNICATION	3	0	0	9	5	0	0	14
		REC 652	COMMUNICATION LAB II	0	0	2		0	0	4	
		REC 601	MICROWAVE ENGINEERING	3	0	0		4	2	0	
12	Prof. Kamakshi	NEC 801	WIRELESS & MOBILE COMMUNICATION	3	1	0	9	5	0	0	15
		REC 651	MICROWAVE ENGG LAB	0	0	2		0	0	4	
		NEC 044	ADVANCE DEGITAL DESIGN USING VHDL	3	1	0		5	0	0	
13	Prof. Ravi Kumar	RIC 603	CONTROL SYSTEM -1	3	0	0	9	5	0	0	14
		RIC 653	CONTROL SYSTEM LAB-1	0	0	2		0	0	4	
1		NEC 044	ADVANCE DEGITAL DESIGN USING VHDL	3	1	0		5	0	0	
14	Prof. Neerai Jain	RAS 601	INDUSTRIAL MANAGEMENT (CS2 & CS3)	6	0	0	13	6	0	0	14
	,,,	RAS 601	INDUSTRIAL MANAGEMENT (2CS)	3	0	0		3	0	0	
		REC 601	MICROWAVE ENGINEERING	3	1	0		4	2	0	
		REC 651	MICROWAVE ENGG LAB	0	0	2		0	0	4	
15	Prof. Arjun Singh Katiyar	RAS 601	INDUSTRIAL MANAGEMENT (CS1)	3	0	0	12	3	0	0	16
		RUC 601	CYBER SECURITY	3	0	0		3	0	0	
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16	Prof VK Agrawal	REC 405	INTRODUCTION TO MICROPROCESSOR (CSE DEPT)	З	0	0	8	5	0	0	14
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	and the second second	REC 403	ELCTRONIC MEASUREMENT & INSTRUMENTATIONS (EC2)	3	0	0		4	0	0	
17	Prof. Arashdeep Kaur	REC 453	ELCTRONIC MEASUREMENT & INSTRUMENTATIONS LAB	0	0	2	11	0	0	4	15
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^p rof. Kamakshi	⁹ rof Dhaarna Arora	Prof Arjun Singh Kat	Prof. Abhishek Sharr	Prof. Praveen Kuma	Prof. Neeraj Jain		Faculty Name		LUE SVN	NEC-352	NEC-354	NEC 303		2 PCB B1	(LDL) BZ		NEC 301	11:30-12:20	4		CLAS					
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Prof. Dhaarna Arora	Optical Communication & Networking Lab	NEC 751	R.N. Baral	Prof. F	1	tip Development	Entrepreneursf	NOE-071
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NOE-071	Entrepreneurship Development	Prof. Pooja Goel	NEC 751	Optical Communication & Networking Lab	Prof. Arjun Singh Katiyar
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NEC 031	Information Theory & Coding	Prof. V K Aggarwal	NEC 752	Electronic Circuit Design lab	Prof. R.N. Baral
NEC 304		Prof Arium Singh Katiwaz			
NEC 701	Optical Communication	Prot. Arjun Singn Katiyar	NEC 753	Industrial Training & Viva Voce	Prof. Kamakshi
NEC 702	Data Communication Networks	Prof. Kamakshi	NIEC 754	Project	Prof. Arjun Singh Katiyar
NEC 703	VLSI Design	Prof. Pankaj Goel			

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Class Cordinator: Prof. V.K Aggarwal

Subj. Code	Subject Name	Faculty Name	Lab Code	Lab Name	Faculty
NOE-071	Entrepreneurship Development	Prof. Pooja Goel	NEC 751	Optical Communication & Networking Lab	Ravi Kumar
NEC 031	Information Theory & Coding	Prof. V K Aggarwal	NEC 752	Electronic Circuit Design lab	Prof. Pooja Goel
NEC 701	Optical Communication	Prof. Ravi Kumar	NIEC 753	Industrial Training & Viva Voce	Prof. Ravi Kumar
NEC 702	Data Communication Networks	Prof. Kamakshi	NEC 754	Project	Prof. V.K Agganwal
NEC 703	VLSI Design	Prof. Pankaj Goel			

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IMS Engineering College IMSEC/OF/08a FORMAT Page 1 of 1 FORMAT Issue No: 01 Class Time Table: Third Year (EC2) Issue No: 01 Prepared By: MR CLASS TIME TABLE FOR ECE W.E.F. 02/08/2016 Academic Session 2016-17 (ODD) . Academic Session 2016-17 (ODD) .	11	10	6	8	7	6	ъ	4	3	2	1	DAY/TI
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NEC 081	NCER	Prof. Pankai Goel		
NEC 802	OPTICAL NETWORK	PROF Manish Zadoo		
NEC 041	ELECTRONIC SWITCHING	Prof. Dhaarna Arora		
NEC 801	IRELESS & MOBILE COMMU	Prof. Balwant Singh		
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NEC 802	OPTICAL	NETWORK	PROF Mani	ish Zadoo					
NEC 041	ELECTRONIC	SWITCHING	Prof. Dhaa	rna Arora					
NEC 801	IRELESS & M	OBILE COMMU	Prof. Balwa	ant Singh					
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MON		NEC 802 2EC	NEC 801	NEC 081 2EC	NEC 802 2EC	NEC 041 2EC			
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COURSE FILE

OF

Integrated Circuits (KEC 501)

2020-2021

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

IMS ENGINEERING COLLEGE, GHAZIABAD

Faculty Name: Praveen Kumar

Branch: Electronics and Communication Engineering

Semester: 5th

Session: 2020-21

Subject Name: Integrated Circuits

Subject Code: KEC 501

IMS ENGINEERING COLLEGE	IMSEC/QF/42
	Page 1 of 1
FORMATS	Issue No: 02
Course File Cover Page	Issue Date: 1 May 2010
Prepared by: MR	Approved by: Director

	Particulars
1.	Quality Policy (on left inside cover of Course File)
2.	Institute Mission and Vision
3.	Departmental Mission and Vision
5.	Program Outcomes (PO)
6.	Program Educational Objectives (PEO) and Program Specific Outcomes (PSO)
7.	Academic Calendar
8	Time Table
9	Student List
10.	University Evaluation Scheme
11.	Syllabus (Theory)
12.	Course Outcome, Mapping with PO/PSO
13.	Syllabus (Practical) with Experiment List mapped with Course Outcomes
14.	Topics beyond Syllabus
15.	Quiz/Assignment/Tutorial Records
16.	CT Question Paper (mapped with CO)
17.	Sessional Marks Analysis
18.	Lecture Notes/PPT
19.	Question Bank
20	Last three years University Question Paper (AKTU) with Solution
21	Attendance Register

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Department of Electronics and Communication Engineering

Vision of the Institution

Our vision is to impart vibrant, innovative and global education to make IMS the world leader in terms of excellence of education, research and to serve the nation in the 21st century.

Mission of the Institution:

- To develop IMSEC as a centre of Excellence in Technical and Management education.
- To inculcate in its students the qualities of Leadership, Professionalism, Executive competence and corporate understanding.
- To imbibe and enhance Human Values, Ethics and Morals in our students.
- To transform students into Globally Competitive professionals.

Vision (Department):

To produce highly competent engineers by imparting innovative and accomplished information through global education and adequately prepare them to face the challenges of outside world by fulfilling the requirements of Electronics & Communication industries.

Mission (Department):

- To make the department a centre of excellence in Electronics & Communication Engineering and to produce eminent engineers.
- > To inculcate professionalism, team work, leadership qualities by imbibing high human values and professional ethics, in students.
- To enhance the employability of students by giving inter-disciplinary knowledge to meet the need of society and become globally competitive professionals.
- To become a centre for research in the stream of Electronics & Communication Engineering and to provide excellent learning environment for researchers by promoting research activities in the department.

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Department of Electronics and Communication Engineering

PROGRAM OUTCOMES (POs)

- 1. Engineering knowledge: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization for the solution of complex engineering problems.
- Problems analysis: Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
- Design development and solutions: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for public health and safety and cultural, societal and environmental considerations.
- Conduct investigations of complex problems: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
- 5. Modern tool usage: Create, select, and apply appropriate techniques, resources and modern engineering IT tools, including prediction and limitations.
- 6. The engineer and society: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
- 7. Environment and sustainability: Understand the impact of the professional engineering solutions in societal and environmental contexts and demonstrate the knowledge of and need for sustainable development.
- 8. Ethics: Apply ethical principles, commit to professional ethics, responsibilities and norms of the engineering practice.
- 9. Individual and team work: Function effectively as an individual, as a member or leader in diverse teams and in multidisciplinary settings.
- 10. Communication: Communicate effectively on complex engineering activities with the engineering community and with the society at large. To be able to comprehend and write effective reports, design documentation, make presentations, give and receive clear instructions.
- 11. Project management and finance: Demonstrate knowledge, understanding of the engineering and management principles. Apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
- 12. Life-long learning: Recognize the need for and have the preparation, ability to engage in independent and life-long learning in the broadest context of technological change.

Department of Electronics and Communication Engineering

Program Educational Objectives (PEOs)

- PEO1: Graduates will excel in Electronics & Communication Engineering, both in industrial and academic sector by applying their technical skills and knowledge in a professional manner.
- PEO2: Graduates will be capable of effectively analyzing and solving engineering problems utilizing appropriate techniques and advanced engineering tools.
- PEO3: Graduates will be capable of applying their knowledge both in individual and multidisciplinary environments. They will also demonstrate excellent communication skills and caliber to work as a team.
- PEO4: Graduates will realize the significance of environmental concerns while keeping safety, ethical and societal values into consideration.
- PEO5: Graduates will be capable of implementing outputs derived from research based knowledge in projects, analysis and interpretation of data leading to development of new processes and systems.

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Department of Electronics and Communication Engineering

PROGRAM SPECIFIC OUTCOMES (PSOs)

At the end of the program, the students will have:

- An ability to exhibit knowledge acquired from mathematics, engineering fundamentals, Electronics & Communication engineering and related fields for professional excellence in industry and research organizations.
- An ability to solve and communicate complex Electronics and Communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive at cost effective and appropriate solutions.
- Wisdom of social and environmental awareness along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using aptimal resources as an Entrepreneur.
- An ability to select appropriate techniques, resources for execution of projects and function effectively as an individual as well as a team member in multidisciplinary diverse environments.

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IMS ENGINEERING COLLEGE, GHAZIABAD ACADEMIC CALENDAR (As per AKTU) (ODD SEM: 2020 - 21) [Version-1]

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		leen	neel	Apr	-2 4th YEAR (C-306)	sion2020-21(ODD)	Period-4	12:00-12:50					KEC-501		Lab Name	Electronics Devices Lab	Integrated Circuits Lab
IMSEC/QF/08b	rage 1 01 1	a Date: 1 May 2010	C Date: T Migh FOTO	proved by: Director			Break	12:50-2:00 PM									
							Period-5	2:00-2:50 PM	Electronics	Integrate		KEC-501					
							Period-6	3:00-3:50 Ph	s Devices Lab	- iteration							

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IMS ENGINEERING COLLEGE GHAZIABAD ELECTRONICS & COMMUNICATION ENGINEERING DEPARTMENT EC 3rd year

S.No.	Roll No.	Name	Student No.	Father No.
1	1714331042	RAHUL SINGH	8512846443	
2	1814331002	AASHI SINGH	9760844799	7253090799
3	1814331004	ABHISHEK KANDPAL	8929297923	9810334103
4	1814331003	ABHISHEK KUMAR	7352133304	9348555526
5	1814331005	ADITYA KUMAR	7524056794	9598271523
6	1814331006	ADITYA PANDEY	9628647442	9005808762
7	1814331007	AKHIL RUHELA	7838954908	9953004133
8	1814331008	AKSHAY VERMA	7017889514	9410267058
9	1814331009	ALI MAJAZ	8191919749	9634371978
10	1814331010	AMAN SAIFI	9897940786	9897940786
11	1814331011	ANIRUDH MANOJ	8006060404	8006060404
12	1814331012	ANMOL SHARMA	8588861488	9871589567
13	1814331013	ANSHUL SHARMA	9899062918	7428572447
14	1814331014	ANTRIKSH SAXENA	8057290569	9639971946
15	1814331015	ANUBHAV SINGH	9536712418	6396061138
16	1814331016	ARBAZ AKHTAR	7905325543	9540080461
17	1814331028	ARMAN SHAH	9910636028	9958139757
18	1814331017	ARPIT SONI	7607524723	8423002715
19	1814331018	ASHISH CHAUDHARY	7453039250	9719057509
20	1814331019	ASHISH SHARMA	9105212161	9927365600
21	1814331020	AYUSH SAINI	7060050264	9368007688
22	1814331021	HARDIK RASTOGI	8265983373	9837048602
23	1814331022	HARSH JAISWAL	7651966994	9450630124
24	1814331023	JATIN AGARWAL	8171008360	9897046125
25	1814331024	JATIN RANA	9311663355	9871022960
26	1814331025	JAYA SINHA	9354773714	8966841669
27	1814331026	KRITIKA NATH	7530845511	0071001758
28	1814331032	MANIK CHOUDHARY	8082640017	0055072602
29	1814331027	MANSI SAXENA	9794790063	9055072582
30	1814331029	MUDIT PRATAP SINGH	9415908182	9044879071

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31	1814331030	MUKUL CHAUHAN	8859977600	8859977600
32	1814331031	MUNESH KUMAR SINGH	7007912346	9952709172
- 33	1814331033	NIKHIL KUMAR	8192828586	9410653845
34	1814331034	NISHA .	9821151993	9716598366
35	1814331035	NITESH UPADHYAY	8006041323	8006041323
36	1814331036	PRABHAT MITTAL	9457625151	9410224751
37	1814331037	PRADEEP DUBEY	9598900234	7532989975
38	1814331038	PRAKHAR TRIVEDI	9554604065	9415474508
39	1814331039	RACHIT GARG	9717182905	9667223326
40	1814331040	RISHABH GUPTA	7081168512	9026374265
41	1814331041	RIYA AGARWAL	9412659808	9837654012
42	1814331042	SAKSHI VARSHNEY	7455007178	9058464594
43	1814331043	SARANSH RAI	9682290100	9532706590
44	1814331044	SARTHAK GUPTA	9784546866	9887859633
45	1814331045	SAURABH GUPTA	8382814157	9984160785
46	1814331046	SHASHWAT DWIVEDI	9161133639	9090973080
47	1814331047	SHELENDRA RAGHAV	9868937012	8130603668
48	1814331048	SHIVAM KATIYAR	9354483513	9654958542
49	1814331049	SHIVANGI MISHRA	9532215002	8800108462
50	1814331050	SUPREET DEOL	8160586479	9927647574
51	1814331051	TANISH VARSHNEY	7906229438	9219758815
52	1814331052	TANISHKA VATS	8810335918	9599612689
53	1814331053	TUSHAR KUMAR	7906365288	7060153909
54	1814331054	UTKARSH SINGH	6351611541	7228888653
55	1814331055	VED PRAKASH SHARMA	9472207260	9631623631
56	1814331056	VISHAL RANA	7839801507	8650664356
57	1814331057	YASH DIXIT	8279724868	9917022660
58	1814331058	YASHASVI SINGH	9956441270	9918164501
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ELECTRONICS AND COMMUNICATION ENGINEERING

S. No.	Course Code	Course Title	P	erio	ls	E	aluat	ion Scher	me	Er	nd ester	Total	Credit
			L	T	P	CT	TA	Total	PS	TE	PE		
1	XEC:501	Integrated Circuits and	3	1	0	30	20	50	0.253	100	1.27	150	4
2	KEC-502	Microprocessor & Microcontroller	3	1	0	30	20	50		100	,	150	4
3	KEC-503	Digital Signal Processing	3	1	0	30	20	50		100		150	4
4	KEC-051-054	Department Elective-I	3	0	0	30	20	50		100		150	3
5	KEC-055-058	Department Elective-II	3	0	0	30	20	50		100		150	3
6	KEC-551	Integrated Circuits Lab	0	0	2				25		25	50	1
7	KEC-552	Microprocessor & Microcontroller Lab	0	0	2				25	*	25	50	1
8	KEC-553	Digital Signal Processing Lab	0	0	2				25		25	50	1
9	KEC-554	Mini Project/Internship **	0	0	2				50			50	1
10	KNC501/KNC502	Constitution of India, Law and Engineering / Indian Tradition, Culture and Society	2	0	0	15	10	25		50			NC
11		MOOCs (Essential for Hons. Degree)											
		Total										950	22

B.Tech. V Semester

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Course Code

Course Title

	Department Elective-I
KEC-051	Computer Architecture and Organization
KEC-052	Industrial Electronics
KEC-053	VLSI Technology
KEC-054	Advance Digital Design using Verilog
	Department Elective-II
KEC-055	Electronics Switching
KEC-056	Advance Semiconductor Device
KEC-057	Electronics Measurement & Instrumentation
KEC-058	Optical Communication

Curriculum & Evaluation Scheme (V & VI semester)

Page 2

ELECTRONICS AND COMMUNICATION ENGINEERING

3L:1T:0P

4 Credits

INTEGRATED CIRCUITS

KEC-501 Lectures Unit Topics The 741 IC Op-Amp: General operational amplifier stages (bias circuit, the input 8 stage, the second stage, the output stage, short circuit protection circuitry), device parameters, DC and AC analysis of input stage, second stage and output stage, gain, frequency response of 741, a simplified model, slew rate, relationship between ft and slew rate. 11 Linear Applications of IC Op-Amps: Op-Amp based V-I and I-V converters, 8 instrumentation amplifier, generalized impedance converter, simulation of inductors. Active Analog filters: Sallen Key second order filter, Designing of second order low pass and high pass Butterworth filter, Introduction to band pass and band stop filter, all pass active filters, KHN Filters. Introduction to design of higher order filters. 111 Frequency Compensation & Nonlinearity: Frequency Compensation, Compensation 4 of two stage Op-Amps, Slewing in two stage Op-Amp. Nonlinearity of Differential Circuits, Effect of Negative feedback on Nonlinearity. Non-Linear Applications of IC Op-Amps: Basic Log-Anti Log amplifiers using 8 diode and BJT, temperature compensated Log-Anti Log amplifiers using diode, peak detectors, sample and hold circuits. Op-amp as a comparator and zero crossing detector, astable multivibrator & monostable multivibrator. Generation of triangular waveforms, analog multipliers and their applications. Digital Integrated Circuit Design: An overview, CMOS logic gate circuits basic IV 6 structure, CMOS realization of inverters, AND, OR, NAND and NOR gates. Latches and Flip flops: the latch, CMOS implementation of SR flip-flops, a simpler CMOS implementation of the clocked SR flip-flop, CMOS implementation of J-K flipflops, D flip- flop circuits. Integrated Circuit Timer: Timer IC 555 pin and functional block diagram, 6 Monostable and Astable multivibrator using the 555 IC. Voltage Controlled Oscillator: VCO IC 566 pin and functional block diagram and applications. Phase Locked Loop (PLL): Basic principle of PLL, block diagram, working, Ex-OR gates and multipliers as phase detectors, applications of PLL.

Text Book:

0

- 1. Microelectronic Circuits, Sedra and Smith, 7th Edition, Oxford, 2017.
- 2. Behzad Razavi: Design of Analog CMOS Integrated Circuits, TMH

Reference Books:

- 1. Gayakwad: Op-Amps and Linear Integrated Circuits, 4th Edition Prentice Hall of India, 2002.
- 2. Franco, Analog Circuit Design: Discrete & Integrated, TMH, 1st Edition.
- 3. Salivahnan, Electronics Devices and Circuits, TMH, 3rd Edition, 2015
- 4. Millman and Halkias: Integrated Electronics, TMH, 2nd Edition, 2010

Course Outcomes: At the end of this course students will demonstrate the ability to:

- 1. Explain complete internal analysis of Op-Amp 741-IC.
- 2. Examine and design Op-Amp based circuits and basic components of ICs such as various types of filter.
- 3. Implement the concept of Op-Amp to design Op-Amp based non-linear applications and wave-shaping circuits.
- 4. Analyse and design basic digital IC circuits using CMOS technology.
- 5. Describe the functioning of application specific ICs such as 555 timer, VCO IC 566 and PLL.

Curriculum & Evaluation Scheme (V & VI semester)

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 \leftarrow **OneNote for Windows 10** Class Notebook Home Shapes 🔄 Ink to Shape 🖧 Ink to Text 5 1ÅI 001 Lecture No 17 Error correction possible 9 18 September 2020 6 Hamming Code Hamming code is an error-correcting code. It is constructed by adding a number of parity bits to each group of *n*-bit information, or message in such a way so as to be able to locate the bit

position in which error occurs. Let us assume that k parity bits $p_1, p_2, ..., p_k$ are added to the *n*-bit message to form an (n + k)-bit code. The value of k must be chosen in such a way so as to be able to describe the location of any of the n + k possible error bit locations and also 'no error' condition. Consequently, k must satisfy the inequality

$$2^k \ge n + k + 1. \tag{2.2}$$

The location of each of the n + k bits within a code word is assigned a decimal number, starting from 1 to the *MSB* and n + k to the *LSB*. k parity checks are performed on selected bits of each code word. Each parity check includes one of the parity bits. The result of each parity check is recorded as 1 if error has been detected and as 0 if no error has been detected. Let the results of the parity checks involving the parity bits p_k, p_{k-1}, \ldots are c_1, c_2, \ldots respectively. Bit c_1 is 1 if an error is detected and 0 if there is no error. Similarly c_2, c_3, \ldots , etc. The decimal value of the binary word formed c_1, c_2, \ldots, c_k gives the decimal value assigned to the location of the erroneous bit. If there is no error, then the decimal value will be 0. This decimal number is the position or location number. The parity bits p_1, p_2, \ldots are placed in locations 1, 2, 4, \ldots , 2^{k-1} .





Values (0 or 1) are assigned to the parity bits so as to make the Hamming code have either even parity or odd parity and when an error occurs, the position number will take on the value assigned to the location of the erroneous bit.

In the case of BCD code with three parity bits there are seven error positions. Table 2.13 gives these error

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IMS Engli Department of Elect * Required 1. Email address *	neering College Ghaziabad	 A D flip flop can be constructed from which flip flop by using an additional 1 point NOT gate. * Mark only one oval. S-R Both J-K and S-R J-K T
Quiz		 Determine the characteristic equation of T flip flop? ¹ point Mark only one oval.
Subject Name :-Dig Subject Code :- KEC 302	gital System Design	$Q_{n+1}=T_{n-}Q_{n'}+T_{n'}Q_{n}$ $Q_{n+1}=T_{n-}Q_{n}+T_{n'}Q_{n}$
2. Roll No. *		Qn+1=Tn + Tn'.Qn
3. Name *		 Which of the following flip flop is not free from race around condition? * 1 point Mark only one oval.
Important Instructions	 All questions are compulsory. Each question carry one mark. You are allowed to submit only once, therefore verify your answers before submission. Do not submit using multiple email ids, this may lead to cancellation of your exam. 	 D Flip Flop T Flip Flop JK Flip Flop Master Slave JK Flip Flop

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1 point

IMS Engineering College Ghaziabad

 $https://docs.google.com/forms/d/1_-y3B3B1fcuwCXDEBkrb64TsOAi... \quad IMS \ Engineering \ College \ Ghaziabad \qquad and \ College \ Ghaziabad \qquad and \ College \ Ghaziabad \ Ghaziabad \ College \ College \ College \ College \ Co$

1 point

https://docs.google.com/forms/d/1_-y3B3B1fcuwCXDEBkrb64TsOAi...

Consider the following state table:

Present	Next	Next state		tput	
state	$\mathbf{X} = 0$	X = 1	X = 0	X=1	
a	a	b	0	1	
b	c	d	0	0	
с	a	d	0	1	
d	e	f	1	0	
e	a	f	1	0	
f	g	f	1	0	
g	a	f	1	0	

Which of the following statements are TRUE?

- I. The state table corresponds to a Mealy Machine.
- II. The number of states can be reduced to a minimum of 5 states.
- III. The number of states can be reduced to a minimum of 6 states.
- IV. States 'd', 'e', 'f' and 'g' are equivalent.
- V. States 'd' and 'f' are equivalent.

Mark only one oval.

- 🔵 III, IV, V only
- 🔘 I, III, IV only
- 🔘 I, II, V only
- 🔵 II, IV, V only

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The waveform indicates the operation of



Mark only one oval.

8. Question *

- Negative edge triggered J-K Flip Flop
- Positive edge triggered S-R Flip Flop
- Positive edge triggered D Flip Flop
- ONegative edge triggered T Flip Flop

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17. The following is a circuit of *

ECL NOR/OR gate CMOS NOR/OR gate

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15-01-2021, 12:08

IMS ENGINEERING COLLEGE		IMSEC/QF/48	
		Page 1 of 1	
FC	ORMATS	Issue No: 02	
Tutorials/ As	signments/ Quizzes	Issue Date: 1 M	ay 2010
Prepared by: MR		Approved by: I	Director
Subject Name	: Integrated Circuits	Subject Code	REC-501
Date of Handout	: 09-08-2019	Max Marks	
Date of Submission	:14-08-2019		

- **Q.1.** Explain MOSFET current mirror, also show the effect of V_0 on I_0 .
- **Q.2.** Describe BJT current mirror and show the effect of finite β on the Current transfer ratio.
- **Q.3.** For $V_{dd} = 1.8V$ and using $I_{REF} = 50\mu A$. It is required to design the circuit of following fig. to obtain an output current whose nominal value is $50\mu A$. Find R if Q_1 and Q_2 are matched with channel lengths of $0.5\mu m$, channel widths of $5\mu m$, $V_t = 0.5V$ and $k_n' = 250\mu A/V^2$. What is the lowest possible value of V_0 ? Assuming that for this process technology the early voltage $V'_A = 20V/\mu m$, find the output resistance of current source.

Q.4. Following Fig. shows an N output current mirror. Assuming that all transistors are matched and have finite β and ignoring the effect of finite output resistances, show that

For $\beta = 100$, find the maximum number of outputs for an error not exceeding 10%.

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		Page 1 of 1	
FOI	RMATS	Issue No: 02	
Tutorials/ Assi	ignments/ Quizzes	Issue Date: 1 May	2010
Prepared by: MR		Approved by: Dir	rector
Subject Name	: IC	Subject Code	REC-501
Date of Handout	: 16.08.2019	Max Marks	
Date of Submission	: 23.08.2019		

- Q.1. Explain Wilson MOS mirror. Also draw the circuit of improved Wilson mirror.
- **Q.2.** Draw the circuit of a bipolar mirror with base current compensation. Explain how it reduces the effect of β on current transfer ratio of current mirror.
- **Q.3.** Explain the cascode current mirror. Write the advantage and disadvantage of the cascode current mirror.
- **Q.4.** Explain Widlar current source. Following figure (a) and (b) shows the two circuit for generating a constant current of 10μ A which operates from 10V supply. Determine the value of required resistors assuming that $V_{BE} = 0.7V$ at a current of 1mA and neglecting the effect of finite β .

IMS ENGINEE	RING COLLEGE		IMSEC/QF/48		
			Page 1 of 1		
FOF	RMATS		Issue No: 02		
Tutorials/ Assignments/ Quizzes			Issue Date: 1 May 2010		
Prepared by: MR			Approved by: Direc	ctor	
Subject Name	: Integrated Circuits	Sı	ibject Code	REC-501	
Date of Handout	: 30-09-2019	Μ	ax Marks		
Date of Submission	: 09-09-2019				

- Q.1 Draw the circuit diagram of CMOS inverter and explain its transfer characteristics.
- Q.2 List the advantage of CMOS logic family
- Q.3 Draw the CMOS realization of the following Boolean expression

a) $Y = \overline{A + B(C + D)}$	b) $Y = \overline{(A+B).C+D}$	
c) $Y = \overline{A + (B + C) + D.E}$	d) $Y = AB + \overline{A}\overline{B}$	e) $Y = AB + C$

- **Q.4** Discuss the features of CMOS circuit. Realize one AND-OR-INVERT (AOI) and one OR- AND-INVERT (OAI) function using CMOS logic circuit.
- **Q.5** Design a CMOS full adder circuit with three inputs A, B, C and two output S and C₀.
- **Q.6** Give a CMOS logic circuit that realizes the function of three input odd parity checker. Specificially, the output is to be high when an odd number (1 or 3) of the input are high. Attempt a design with 10 transistors (not counting those in the inverters) in each of the PUN and PDN.

IMS ENGINEI	ERING COLLEGE	IMSEC/QF/48	
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FO	RMATS	Issue No: 02	
Tutorials/ Ass	ignments/ Quizzes	Issue Date: 1 May 2	010
Prepared by: MR		Approved by: Direc	tor
Subject Name	: Integrated Circuit	Subject Code	REC-501
Date of Handout	: 13-09-2019	Max Marks	
Date of Submission	: 19-09-2019		

- **Q.1** For a process technology with L=0.5µm, n=1.5, p=6. Give size of all transistors in (i) a four input NOR and (ii) a four input NAND Gate. Also compare the area of two Gates and then shows that CMOS NAND is preferred over CMOS NOR.
- Q.2 Determine the W/L ratios for all transistor used in CMOS implementation of the function $Y = \overline{A(B + CD)}$
- **Q.3** Give the CMOS implementation of clocked SR flip-flop and explain its working.
- **Q.4** Draw the D-flip flop using CMOS. Also draw and explain its master slave configuration.

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FOI	RMATS	Issue No: 02	
Tutorials/ Ass	ignments/ Quizzes	Issue Date: 1 May	2010
Prepared by: MR		Approved by: Dire	ector
Subject Name	: Integrated Circuit	Subject Code	REC-501
Date of Handout	: 27-09-2019	Max Marks	
Date of Submission	: 03-10-2019		

- **Q.1** Define the following term with reference to op-amp
 - (i) CMRR (ii) Slew rate (iii) PSRR
 - (iv) Input offset voltage (v) Bias current
- **Q.2** Realize generalized impedance converter (GIC) with op-amp. How the inductor is simulated using this GIC.
- **Q.3** Draw a second order low-pass and high pass filter and drive its transfer function. Design a second order low pass butterworth filter having upper cut-off frequency of 1kHz and a passband gain of 2
- **Q.4** Derive the expression of voltage gain in KHN biquad filter.
- Q.5 Draw the following Circuit using op-amp
 - (i) Weighted Summer (ii) Difference Amplifier
 - (iii) V-I converter (iv) I-V Converter

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FOI	RMATS	Issue No: 02		
Tutorials/ Ass	ignments/ Quizzes	Issue Date: 1 May 2010		
Prepared by: MR		Approved by: Dire	ctor	
Subject Name	: Integrated Circuit	Subject Code	REC-501	
Date of Handout	: 18-10-2019	Max Marks		
Date of Submission	: 23-10-2019			

- **Q.1** Draw and explain the circuit of temperature compensated logarithmic amplifier.
- **Q.2** Draw and explain the circuit of temperature compensated anti-logarithmic amplifier.
- **Q.3** Draw and explain the circuit diagram of precision full wave rectifier.
- **Q.4** Explain inverting and non-inverting Schmitt trigger.
- **Q.4** Draw and explain the circuit of square wave generator circuit using op-amp.

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		Page 1 of 1		
FO	RMATS	Issue No: 02		
Tutorials/ Ass	ignments/ Quizzes	Issue Date: 1 May 2010		
Prepared by: MR		Approved by: Direc	tor	
Subject Name	: Integrated Circuit	Subject Code	REC-501	
Date of Handout	: 08-11-2019	Max Marks		
Date of Submission	: 15-11-2019			

- **Q.1** Draw the functional block diagram of IC 555 and explain its working.
- Q.2 Draw and explain monostable multivibrator using 555 timer and calculate its pulse width period.
- **Q.3** Draw and explain astable multivibrator using 555 timer and find the free running frequency of the output.
- Q.4 An 8bit DAC has an input of 10011011 and 10V reference, find the corresponding output voltage.
- Q.5 The basic step of a 8-bit DAC is 20mV. If 00000000 represents 0V, what is represented by the input 10110111.
- **Q.6** Explain the operation of Dual slope ADC.

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(http://52. 66.1d.Dotuster# /dashboard)	Course	B.Tech	~	Stream	Electronics & Communication	>
■ Module (http://52.66.16.110 /user#/module_list)	Year	3 Year	~	Subject	Integrated Circuits (KEC 501)	~
L+ Assignment	Section	EC1	~			
🍨 Assignment						

♣ Student Wise Assignment Report
• Faculty Wise Assignment

Faculty Wise Assignment Report

✤ Section Wise Assignment Report

#	Registered	Batch	Status	Roll No	Student Name	Assignment 07	Assignment 06	Assignment 05	Assignment 04	Assignment 03	Assignment 02	Assignment 01
1	Yes	EC1	Regular	1714331042	RAHUL SINGH	1	0	1	1	1	1	1
2	Yes	EC1	Regular	1814331002	AASHI SINGH	1	1	0	1	1	1	1
3	Yes	EC1	Regular	1814331003	ABHISHEK KUMAR	1	1	1	1	1	1	1
4	Yes	EC1	Regular	1814331004	ABHISHEK KANDPAL	1	1	1	1	1	1	1
5	Yes	EC1	Regular	1814331005	ADITYA KUMAR	1	1	1	1	1	1	0
6	Yes	EC1	Regular	1814331006	ADITYA PANDEY	1	1	1	1	1	1	1
7	Yes	EC1	Regular	1814331007	AKHIL RUHELA	1	1	1	1	1	1	1
8	Yes	EC1	Regular	1814331008	AKSHAY VERMA	1	1	1	0	1	1	1
9	Yes	EC1	Regular	1814331009	ALI MAJAZ	1	1	1	1	1	1	1
10	Yes	EC1	Regular	1814331010	AMAN SAIFI	1	1	1	1	1	1	1
11	Yes	EC1	Regular	1814331011	ANIRUDH MANOJ	0	0	0	1	1	1	1
12	Yes	EC1	Regular	1814331012	ANMOL SHARMA	1	1	1	1	1	1	1
13	Yes	EC1	Regular	1814331013	ANSHUL SHARMA	1	1	1	1	1	1	1
14	Yes	EC1	Regular	1814331014	ANTRIKSH SAXENA	1	1	1	1	1	1	1
15	Yes	EC1	Regular	1814331015	ANUBHAV SINGH	1	1	1	1	1	1	1
16	Yes	EC1	Regular	1814331016	ARBAZ AKHTAR	1	1	1	1	1	1	1
17	Yes	EC1	Regular	1814331017	ARPIT SONI	1	1	1	1	1	1	1
18	Yes	EC1	Regular	1814331018	ASHISH CHAUDHARY	1	1	0	1	1	1	1
19	Yes	EC1	Regular	1814331019	ASHISH SHARMA	1	1	1	1	1	1	1
20	Yes	EC1	Regular	1814331020	AYUSH SAINI	0	1	0	0	1	1	1
21	Yes	EC1	Regular	1814331021	HARDIK RASTOGI	1	1	1	1	1	1	1
22	Yes	EC1	Regular	1814331022	HARSH JAISWAL	1	1	1	1	1	1	1
23	Yes	EC1	Regular	1814331023	JATIN AGARWAL	1	1	1	1	1	1	1
24	Yes	EC1	Regular	1814331024	JATIN RANA	1	1	1	1	1	1	1

	#	Registered	Batch	Status	Roll No	Student Name	Assignment 07	Assignment 06	Assignment 05	Assignment 04	Assignment 03	Assignment 02	Assignment 01	Total
(http://52.66 🎛	1 ²⁵ (۲ ^{Yes}	EC1	Regular	1814331025	JAYA SINHA	1	1	1	1	1	1	1	7
	26	yes	EC1	Regular	1814331026	KRITIKA NATH	1	1	1	1	1	1	0	6
(http://52.66.14.Douser#	27	Yes	EC1	Regular	1814331027	MANSI SAXENA	1	1	1	1	1	1	1	7
	28	Yes	EC1	Regular	1814331028	ARMAN SHAH	1	1	1	1	1	1	1	7
/user#/module_list)	29	Yes	EC1	Regular	1814331029	MUDIT PRATAP SINGH	1	1	1	1	1	1	1	7
⊈ + Assignment	30	Yes	EC1	Regular	1814331030	MUKUL CHAUHAN	1	1	1	1	1	1	1	7
🖢 Assignment	31	Yes	EC1	Regular	1814331031	MUNESH KUMAR SINGH	1	1	0	1	0	1	1	5
와 Student Wise Assignment	32	Yes	EC1	Regular	1814331032	MANIK CHOUDHARY	1	1	1	1	1	1	1	7
Report	33	Yes	EC1	Regular	1814331033	NIKHIL KUMAR	0	1	1	1	1	1	1	6
Faculty Wise Assignment Report	34	Yes	EC1	Regular	1814331034	NISHA .	1	1	1	1	1	1	1	7
+ Section Wise Assignment	35	Yes	EC1	Regular	1814331035	NITESH UPADHYAY	1	1	1	1	1	1	1	7
Report	36	Yes	EC1	Regular	1814331036	PRABHAT MITTAL	1	1	1	1	1	1	1	7
	37	Yes	EC1	Regular	1814331037	PRADEEP DUBEY	1	1	1	1	1	1	1	7
	38	Yes	EC1	Regular	1814331038	PRAKHAR TRIVEDI	1	0	0	0	1	1	0	3
	39	Yes	EC1	Regular	1814331039	RACHIT GARG	1	1	1	1	1	1	1	7
	40	Yes	EC1	Regular	1814331040	RISHABH GUPTA	1	0	1	1	1	1	1	6
	41	Yes	EC1	Regular	1814331041	RIYA AGARWAL	1	1	1	1	1	1	1	7
	42	Yes	EC1	Regular	1814331042	SAKSHI VARSHNEY	1	1	1	1	1	1	1	7
	43	Yes	EC1	Regular	1814331043	SARANSH RAI	1	1	1	1	1	1	1	7
	44	Yes	EC1	Regular	1814331044	SARTHAK GUPTA	1	1	1	1	1	1	1	7
	45	Yes	EC1	Regular	1814331045	SAURABH GUPTA	1	1	1	1	1	1	1	7
	46	Yes	EC1	Regular	1814331046	SHASHWAT DWIVEDI	0	1	1	1	1	1	1	6
	47	Yes	EC1	Regular	1814331047	SHELENDRA RAGHAV	1	0	0	0	1	1	0	3
	48	Yes	EC1	Regular	1814331048	SHIVAM KATIYAR	1	1	1	1	1	1	1	7
	49	Yes	EC1	Regular	1814331049	SHIVANGI MISHRA	1	1	1	1	1	1	1	7
	50	Yes	EC1	Regular	1814331050	SUPREET DEOL	1	1	1	1	1	1	1	7
	51	Yes	EC1	Regular	1814331051	TANISH VARSHNEY	1	1	1	1	1	1	1	7
	52	Yes	EC1	Regular	1814331052	TANISHKA VATS	1	1	1	1	1	1	1	7
	53	Yes	EC1	Regular	1814331053	TUSHAR KUMAR	1	1	1	1	1	1	1	7
	54	Yes	EC1	Regular	1814331054	UTKARSH SINGH	0	1	1	1	1	1	1	6
	55	Yes	EC1	Regular	1814331055	VED PRAKASH SHARMA	1	1	1	1	1	1	1	7
	56	Yes	EC1	Regular	1814331056	VISHAL RANA	1	1	1	1	1	1	1	7

	#	Registered	Batch	Status	Roll No	Student Name	Assignment 07	Assignment 06	Assignment 05	Assignment 04	Assignment 03	Assignment 02	Assignment 01	Total
(http://5266 7	1 7 (Yes	EC1	Regular	1814331057	YASH DIXIT	1	1	0	0	0	0	0	2
$(\Pi \cup \mathcal{V}, \mathcal{V}) \subset \mathcal{V}, \mathcal{V} $	(58) Yes	EC1	Regular	1814331058	YASHASVI SINGH	1	1	1	1	1	1	1	7
(http://52.66.ud.Surger# /dashboard)														

Module (http://52.66.16.110 /user#/module_list)

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🛂 Assignment

🍨 Assignment

♣ Student Wise Assignment Report

Faculty Wise Assignment Report

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IMS ENGINEERING COLLEGE, GHAZIABAD

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MONTHLY REPORT

Syllabus covered and assignment report

Date: $|9-03-15\rangle$ Year/ semester: Section: EC1/EC2/2EC Name of coordinator:

EC2 4th 72 Pravien Kumaz

Subject code	Subject name	Faculty name	Unit covered(%) /total unit	no of assignment	No. of lectures proposed/ held	signature
EEC 801	Mobile & Wircless Comm.	Abhishek Shazma	2.0	3 (Theree)	26	abhrshell
EEC035	Intro. to Radar System	s Kr	2.0	3	31	Jume
EOEOØI	NCER	Mukesh Khandelud	2.0	2	33	\$f
EEC 802	Electromics smitchigne	J.M. Voishishly	2.6	4	30	John
	19.14 anisi 19.14 anisi 19.14		9 000000000	191.,46	NIR.	
	an anna			(116 to SI)		
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Signature Year coordinator

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IMS ENGINEERING COLLEGE, GHAZIABAD

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MONTHLY REPORT

Syllabus covered and assignment report

Date:

Year/ semester: 2nd year/ 4th semester Section: EC1/EC2/2EC Name of coordinator: 0 Key last

Name of coordinator: Akanksha Shukla

Subject	Subject name	Faculta	TT 1.			
code	- adject manie	racuity	Unit	no of	No. of	signature
		name	covered(%)/total	assignment	lectures	
			unit		proposed/	
NEC 102	DI I	0	and the second second		held	
NEC-402	Electronic	Pravien	47.1	1.	20	0
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NDC 100		pumar				1
NEC-408	Electronic	ALASI doch	45.1	,		
	measurement	multicep	75/0	4	99	1
	and	1	1		da	M
	instrumentation	a distance in				A
NEC-404	EMFT	Maniela	- Landerford - Martin			Y
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		Zadiro	101.	7	da.	Ma
NAS-401	Engg.	Coulable.	1			
	Mathematics-	0000000	401.	4	21	der a
100	III		- 1	1	36	o
NEC-401	Data structure	1. 9		and the second second	-	0
		KING	40%	2.	2 -	f. 10
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NHU-402	Industrial	Akonksha.	-			
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AUC-001	Human	Anale" to				•
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	Professional	Rhardwai	40%	4	06	1. Nita
	Ethics	w w w w w w	101		-0	Ann
1		and the second			1	

ula EC-1 (Akamhsha Shukra) Signature

Year coordinator

IMS ENGINEER	ING COLLEGE, GZB			
Sessional Question Paper	IMSEC/QF/49			
	Page 1 of 1			
	Issue no: 02			
	Issue date: 1 May 2010			
1 st Sessional Examinatio	n (CT-1), Odd Sem. 201	9-20		
Subject Name: Integrated Circuits	Subject code	REC 501		
Roll No. of student	Max Marks	30		
	Max time	1:30hrs		
For EC1, EC2 3rd Year	Approved By Director			

Note: Attempt any six questions

$(6 \times 5 = 30)$

- Q.1 What are the desirable characteristics of current mirror circuit? Draw the simple BJT current mirror circuit and derive the expression of current transfer ratio.
- Q.2 For $V_{dd} = 1.8V$ and using $I_{REF} = 50\mu A$. It is required to design the circuit of Fig.1 to obtain an output current whose nominal value is $50\mu A$. Find R if Q_1 and Q_2 are matched with channel lengths of $0.5\mu m$, channel widths of $5\mu m$, $V_t = 0.5V$ and $k_n' = 250\mu A/V^2$. What is the lowest possible value of V_o ? Assuming that for this process technology the early voltage $V_A' = 20V/\mu m$, find the output resistance of current source.

- Q.3 Explain Wilson Current mirror. How the V_{DS} mismatching is avoided by improved Wilson mirror?
- Q.4 Draw the circuit diagram of cascode current mirror; elso write the advantage and disadvantage of cascode current mirror.
- Q.5 Design a CMOS full adder circuit with inputs A, B, C and two output S and C₀.
- Q.6 Sketch the CMOS realization of the following Boolean function-(a) $Y = \overline{(A + B + C).D}$ (b) $Y = \overline{AB} + A\overline{B}$
- Q.7 Sketch the CMOS implementation of SR flip-flop and explain its working.Q.8 Draw the D-flip flop using CMOS. 11
- Q.8 Draw the D-flip flop using CMOS. Also draw and explain its master slave configuration.

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	Cours	e Outcomes and Qu	estion mapping	7 mately	_
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Sessional Ouestion Paper	IMSEC/QF/4	9
	Page 1 of 1	
	Issue no: 02	
	Issue date:1 N	1ay 2010
2 nd Sessional Exam	nation (CT-2), Odd Sem.	2019-20
Subject Name: Integrated Circuits	Subject code	REC 501
Roll No. of student	Max Marks	30
	Max time	1:30hrs
For EC1, EC2 3rd Year	Approved By	Director

Note: Attempt any six questions

(6×5=30)

- Q.1 Draw the generalized impedance converter and derive its impedance equation. Also simulate an Inductor.
- Q.2 Explain how a Schmitt Trigger circuit works with a neat diagram. Design a Schmitt trigger with Vur = 2V, $V_{LT} = -2V$. Assume $\pm V_{sat} = \pm 13V$.
- Q.3 Draw the circuit of Sallen Key filter and derive the expression of its transfer function. Also design the equal component Sallen key high pass filter.
- Q.4 Derive the expression of voltage gain in KHN biquad filter. Draw the KHN biquad filter and drive transfer function of the BPF and LPF from that.
- Q.5 Draw and explain basic logarithmic amplifier. Also explain temperature compensated logarithmic amplifier.
- Q.6 Explain the working of precision full wave rectifier with necessary waveform.
- Q.7 Design a wide band pass filter with $f_l = 500$ Hz, $f_h = 1500$ Hz and a pass band gain of 4. Draw frequency response of band pass filter and find value of Q.
- **Q.8** Design a 2nd order low pass Butterworth filter with cut off frequency of 1 KHz.

		For offic	e use only		
	Course C	utcomes and	Question mapping	matrix	
CO1	CO2	CO3	CO4	CO5	COG
-	Q. 3, 4, 7, 8		Q.2, 5, 6	-	Q.1

IMSENGINEER	INGCOLLEGE,GZB	
Sessional Question Paper	IMSEC/QF/49	
	Page 1 of 1	
	Issue no: 02	
	Issue date:1 May	y 2010
PUT Examinatio	n, Odd Sem. 2019-20	
Subject Name: Integrated Circuits	Subject code	REC 501
Roll No. of student	Max Marks	70
	Max time	3 Hrs
Prepared By: MR	Approved By Di	rector

Note: All sections are compulsory. If require any missing data; then choose suitably.

Section-A

- Q.1 Attempt any seven parts of this question
 - a) What is the advantage of Widlar current source over simple constant current source?
 - b) Define and give significance of Slew Rate.
 - c) Write the advantage of active filter over passive filter?
 - d) What do you mean by a frequency response of a filter circuit?
 - e) Why CMOS NAND is preferred over CMOS NOR?
 - f) Give two application of analog multiplier.
 - g) What is a Super Diode?
 - h) List the application of PLL.
 - i) The basic step of a 8-bit DAC is 20mV. If 00000000 represents 0V, what is represented by the input 10110111.
 - j) What are the advantages of CMOS logic family?

Section-B

Attempt any three questions of this section.

Q.2 Explain Widlar current source.

Following Fig. (a) and (b) shows the two circuit for generating a constant current of 10µA which operates from 10V supply. Determine the value of required resistors assuming that $V_{BE} = 0.7V$ at a current of 1mA and neglecting the effect of finite β .

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(2×7=14)

 $(7 \times 3 = 21)$

- Q.3 Draw the CMOS realization of the following Boolean expression (i) $Y = \overline{A + B(C + D)}$ (ii) $Y = \overline{(A + B).C + D}$
- Q.4 Explain the circuit of following current mirror and also discuss their advantage-(i) Wilson current mirror (ii) Base current compensated current mirror
- Q.5 Explain the following circuit using op-amp (i) Schmitt trigger (ii) Comparator and zero crossing detector
- Q.6 (i) Design a wide band pass filter with $f_L = 200$ Hz, $f_H = 1$ KHz and a pass band gain of 4. (ii) Design a 2nd order Butterworth high pass filter with cut-off frequency of 1KHz.
- Q.7 Explain R-2R ladder type digital to analog converter.

Section-C

Attempt any one part of each questions of this section.

(7×5=35)

- Q.8 a) Discuss the frequency response of 741opamp. Relate unity-gain bandwidth and slew rate.
 b) How the short circuit protection is achieved in the output stage of 741 op-amp?
 c) Explain MOSFET current mirror, also show the effect of V_o on I_o.
- Q.9 a) Draw the circuit of KHN biquad filter and derive the expression of its voltage gainb) Realize generalized impedance converter (GIC) with op-amp. How the inductor is simulated using this GIC.
 - c) Implementation the following filter using op-amp
 - (i) Notch filter (ii) Narrow band pass filter
- Q.10 a) Design a CMOS full adder circuit with three inputs A, B, C and two output S and C_o.
 b) Give the CMOS implementation of clocked SR flip-flop and explain its working.
 c) Draw the D-flip flop using CMOS. Also draw and explain its master slave configuration.
- Q.11 a) Draw and explain the circuit of temperature compensated logarithmic amplifier.
 b) Explain working of precision full wave rectifier with necessary waveform.
 c) Draw and explain the circuit of square wave generator (astable multivibrator) using op-amp and derive the expression of output frequency.
- Q.12 a) Explain the operation of dual slope ADC.
 b) Draw and explain the circuit of astable multivibrator using 555 timer. Also derive the expression of frequency and duty cycle of output wave form.

c) Draw the block diagram of a PLL and explain its operation. Explain lock-in-range, capture range and pull-in time of a PLL.

		For office	e use only		
	Course	Outcomes and Q	Question mapping	g matrix	1.1.1.1.1
C01	CO2	CO3	CO4	CO5	C06
Q.1(a,b), Q.2, Q.4, Q.8	Q.1(c,d), Q.6, Q.9	Q.1(e,j), Q.3, Q.10	Q.1(f, g), Q.5, Q.11	Q.1(i), Q.7, Q.12 (a,c)	Q.1(h), Q.12(b)

IMS Engineering College, Ghaziabad Department of Electronics & Communication Engineering PUT Result Analysis (Odd Semester 2019-20)

Class:	EC1 3rd Year		Sub: 1	Integrated Circu	iits (REC 50
S. No.	University Roll	Name	CT-1 Marks	CT-I Marks (30)	PUT Mark (70)
1	1714331001	ABHISHEK PATEL	12	13	47
2	1714331002	ADARSH KUMAR IHA	12	20	55
3	1714331003	AKSHANSH SINGH	14	AB	35
<u> </u>	1714331004	AMAN KANSAT	12	3	36
4	1714331005	AMAN SINCH ASWAT	12	AD	41
6	1714331005	AMAN DESHWAL	13	AB	71
7	1714331003	AMIT VADAV	12	AB	23
8	1714331007	ANTI SINCH	12	5	37
0	1714331008	ANMOL LATIVAN	12	AB	30
10	1714331009	ANDOD KUNAAD MISUDA	1	AB	1
10	1714331010	ANU SDICH	8	AB	50
11	1714331011	ANUJ SINGH	8	10	33
12	1714331012	ANUSHK SRIVASTAV	19	AB	37
13	1/14331013	ARIHANT JAIN	AB	AB	32
14	1714331014	ASHISH KUMAR DUBEY	15	24	55
15	1714331015	ATUL KUMAR	AB	AB	5
16	1714331016	AYUSH AWASTHI	12	16	35
17	1714331017	CHAKSHU PARASHAR	10	AB	18
18	1714331018	GAURAV THAPLIYAL	0	3	10
19	1714331019	HARSHIT TOMAR	13	AB	28
20	1714331020	HIMANSHU GANGWAR	5	AB	10
21	1714331021	JANMEJAY SINGH CHAUHAN	21	AB	35
22	1714331022	JAYDEEP AGARWAL	23	AB	67
23	1714331023	KARAN SHARMA	13	23	47
24	1714331024	KARTIK SINGHAL	2	2	22
25	1714331025	KM. SHIVANGI AGRAWAL	26	AB	56
26	1714331026	KRISHNA MURARI RAI	5	7	34
27	1714331027	KULDEEP SINGH	12	AB	37
28	1714331029	MEGHA VISHWAKARMA	21	AB	28
29	1714331030	MUDIT GARG	8	AB	40
30	1714331031	MUKUL SINGH SISODIA	4	10	40
31	1714331032	NEERAJ KUMAR	12	AB	23
32	1714331034	NISHI GUPTA	28	AB	3.5
33	1714331035	NITIN KUMAR YADAV	4	AB	48
34	1714331038	PIYUSH KUMAR SINGH	18	4	16
35	1714331075	YATI SHINGAL	28	AB	39
	1			2.3	65
		Number of Students in Section	35	35	35
		Number of Students Present	33	14	35
		No. of Students below 40%	11	8	9
0		Average 240%)	66.67%	42.85%	74.29%
1		Highest Marks Obtained	12.43	11.5	34.8
1,1	Umida I	inguest marks Obtained	28	24	67

(Subject Teacher) Mr. Pravsen Kumar

(Hob/ECE) Prof. (Dr.) R.P.S Chauhan 2 [121]

S ENGINEERING COLLEGE, GHAZIAL D

Department of Electronics & Communication Engineering

Class Average	Overall Pass%	RADAR ENGINEERING	ADVANCE DIGITAL DESIGN USING VERILOG	DIGITAL COMMUNICATION	MICROWAVE ENGINEERING	CONTROL SYSTEM 1	CYBER SECURITY	INDUSTRIAL MANAGEMENT	Subject Name	
		REC 065	REC 064	REC 602	REC 601	RIC 603	RUC 601	RAS 601	Code	Subject
			35	35	35	35		35	Students	S
55.09	91.43	N.A.	58.74	50.40	51.86	56.89	N.A.	58.74	Average	ession: 201
			100	97.14	97.14	100		100	Pass %	17-18
			0	-	H	0		0	CP	
			50	50	50	50	50	50 ·	Students	Se
52.25	84	N.A.	48.97	52.06	52.37	49.34	54.83	55.94	Average	ssion: 201
			92	90	86	90	100	100	Pass %	8-19
			4	S	1	5	0	0	CP	
		13	22	35	35	35	35 .	35	Students	
65		13	22	35	35	35	35	35	Result Declared	Session:
14	00	68.79	65.00	60.45	65.80	66.29	65.59	66.29	Average	2019-20
		100	100	100	100	100	100	100	Pass %	
		0	0	0	0	0	0	0	ę	
65.14	100.00	N,A.	6.26	10.05	13.94	9,40	N.A.	7.55	2017-18	Ava Niff wrt
12.89	16.00	N.A.	16.03	8.39	13.43	16.95	10.76	10.35	2018-19	Ava Diff wrt

Result Analysis for EC1 3rd Year Even Semester 2019-20

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Prof Praveen Chourasia	REC 601	IICROWAVE ENGINEERING
Prof. Myurika Saxena	RIC 603	ONTROL SYSTEM 1
Prof. Sameer Anand (EN)	RUC 601	YBER SECURITY
(ma) farmer managers		
Prof. Sunil Kr Pandev (ME)	RAS 601	VDUSTRIAL MANAGEMENT
Facury Name	Loae	Subject Name
Frank	222	C. Hinnt Namo

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Department of Electronics & Communication Engineering

		Class Average	Overall Pass%		NEC O	RADAR ENGINEERING	USING VERILOG	ADVANCE DIGITAL DESIGN	ADVANCE DIGITAL DESCRIPTION	DIGITAL COMMUNICATION REC.	NEC NEC	MICROWAVE ENGINEEDING DEC	COMINGESTSTEM I RIC	CONTROL EVENENT	CYBER SECURITY RUC	in the second se	INDUSTRIAL MANAGEMENT RAS	6	Subject Name	Subject New Sub
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	30.24		95.65		N.A.		60.56		77'4.0	54.33	56.04		56.89		NA	27.90	10 22	its Average		Session: 20
							100		91.82	0700	100		100			001	100	Pass %		17-18
							0 50		1 50		0 50	00	0 50	00	3	0 50.		CP Students		S
1.110	53.50		88		N.A.		48.74		50.31		51 37	J.T.7/	54 57	76.90	1003	57.06		Average		ession: 2018
A DESCRIPTION OF TAXABLE PARTY.							96 2		94 3	UT U	04 2	U DOT	100	100 0		100 0		Pass % CP		3-19
					13	1	23		36	00	20	36	2	36 .		25		Students		
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				DO DOT	100	001	100 0	0 00T	100	100 0		100 0	TOT	100	100 0		T 455 70 L	Dann Br		
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12.78	12.00	1200		N.A.		18.34		16.20		14.74	11.10	11 70	7.06	1	9.45		51-8107	AVg Diff. WIT		

Result Analysis for EC2 3rd Year Even Semester 2019-20

Prof. Arjun Singh Katiyar	REC 065	ADAR ENGINEERING
Prof. Pankaj Goel	REC 064	ADVANCE DIGITAL DESIGN JSING VERILOG
Prof. Balwant Singh	REC 602	DIGITAL COMMUNICATION
Prof. Praveen Chourasia	REC 601	VICKOWAVE ENGINEERING
Prof. Praveen Kumar	RIC 603	LON I ROL SYSTEM 1
Prof. Sameer Anand (EN)	RUC 601	LTBER SECURITY
Prof. Sunil Kr Pandey (ME)	RAS 601	INDUS I RIAL MANAGEMENT
Faculty Name	Code	subject Name

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