Supporting Document

1.1.1 The Institution ensures effective curriculum delivery through a well-planned and documented process.

IMS ENGINEERING COLLEGE, GHAZIABAD

ACADEMIC CALENDAR (As per AKTU) (ODD SEM: 2020 - 21) [Version-1]

Oct-20						
M	T	W	T	F	S	S
			1	2	3	4
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30	31	
T/ W Days : 19/21						

Nov-20						
M	T	W	T	F	S	S
						1
2	3	4	5	6	7	8
9	10	11	12	13	14	15
16	17	18	19	20	21	22
23	24	25	26	27	28	29
30						
T/ W Days : (16+3)/20						

Dec-20						
M	T	W	T	F	S	S
	1	2	3	4	5	6
7	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29	30	31			
T/ W Days : 17/24						

Jan-21						
M	T	W	T	F	S	S
				1	2	3
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29	30	31
T/ W Days : 15/22						

Feb-21						
M	T	W	T	F	S	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
T/ W Days : 20/22						

Mar-21						
M	T	W	T	F	S	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				
T/ W Days : 5/23						

IMPORTANT DATES	HOLIDAYS	EXAMINATION / CLASS TEST
Commencement of Classes for 2nd, 3rd & 4th Yr: 5th Aug	**14, 15 & 16 NOV (SAT, SUN & MON):** Deepawali	CT-1 : **2nd-DEC to 8th-DEC, 2020**
Commencement of Classes for 1st & 2nd (Lateral) 25th NOV	**30-NOV (MON) :** Guru Nanak's B'day	CT-2 : **19, 21, 26, 28-DEC, 2, 4 JAN 2021**
	25-DEC (FRI) : Christmas Day	PUT : **18th JAN to 23rd JAN, 2021**
	11-MAR (THU) : Maha Shivratri	**(3rd & 4th Year AKTU External)**
Upload Assignment (Important Dates)	**28-MAR (SUN) :** Holika Dahen	**AKTU** End Sem Exam (01-FEB to 20-FEB, 2021)
	29-MAR (MON) : Holi	**(1st & 2nd Year AKTU External)**
		AKTU End Sem Exam (08-MAR to 20-MAR, 2021)
		AKTU End Sem Practical Examination

Total Teaching Days/Working Days (T/W) : 60/132 [95/132]

Faculty members are requested to 1) Upload the attendance after completion of the class (L/T/P) itself on the same day.
2) Upload / Check / Submit the assignment as per schedule (weekly).

...S ENGINEERING COLLEGE, GHAZIABAD

CENTRAL LIBRARY

BOOKS REQUISITION FORM

Date: 10/1/18 (2017-18)

To
The Director Sir
IMSECS, Ghaziabad
Respected Sir

Course: (B.Tech/MBA/MCA/M.Tech)
Branch: ECE
Year/Semester:

It is recommended that the following books may be purchased for the college library. Sanction for purchase may please be accorded.

S.No.	Author	Title	Publication	Copies Reqd.	No. of Students	Existing copies	Appx. Price	Amt. (INR)
1.	T.R. Padmanabhan & B. Bala Tripura Sundari	"Design through verilog HDL"	Wiley Publication	~~100~~ 25	120	24 (older) Samir Patnaik	579 (J. Pe)	57900
2.	John H. Davies	MSP430 Microcontroller basics 1st edition	Newnes Publication	102	101	NIL	525/- Per Copy	53550/-

1. Subject: NEC 024R Advance digital system design using verilog — Teacher (s): Sujeet Kumar, Rajiv Kumar
2. REC-401 microprocessor & microcontroller

both new subjects

HOD

Dean (Academics) 10/1/18

Librarian

Director Sir

Rajiv Kr

Rajeev Agarwal

6 Hrs

4 Hrs

IMS ENGINEERING COLLEGE, GHAZIABAD
CENTRAL LIBRARY
BOOKS REQUISITION FORM

Date: 15/12/2016 (2016-17)
Course: (B.Tech/MBA/MCA/M.Tech)
Branch: IT
Year/Semester: IIIrd yr (VIth Sem).

To
The Director Sir
IMSECS, Ghaziabad
Respected Sir

It is recommended that the following books may be purchased for the college library. Sanction for purchase may please be accorded.

S.No.	Author	Title	Publication	Copies Reqd.	No. of Students	Existing copies	Appx. Price	Amt. (INR)
01	Roger Pressmen	Software Engineering	MGH	91	91	XII L	795/-	
02	Efraim Turban	Knowledge based Decision Support Systems business intelligence.	Pearson	57	91	34	799/-	
03	Dr Seema Acharya	Big Data Analytics	willey	91	91	XII L	539/-	
04	Aho, Lam Sethi, Ullman	Compiler Degin	Pearson	61	91	30	899/-	
05.	Shanmugham, K. Sam	Digital & Analog communication Systems	Wiley	110	102	91	619/-	

Subject:
1 Big Data
2 KBDSS
3 Software Engg
4 Compiler

Teacher (s):
1. Dr S N Rajan
2. Prof Updesh Tiwari
3. Prof Upender Nishtha
4. [illegible]

HOD 15/12/16

20.12.16.
Dean Academics

Librarian 15/12/16

Director Sir

Updesh 13/12/16

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CENTRAL LIBRARY
BOOKS REQUISITION FORM

Date: 8/12/15 (2015-16)
Course: (B.Tech/MBA/MCA/M.Tech)
Branch: I T
Year/Semester: 4th Semester

(Increase Intake IT)

To
The Director Sir
IMSECS, Ghaziabad
Respected Sir

It is recommended that the following books may be purchased for the college library. Sanction for purchase may please be accorded.

S.No.	Author	Title	Publication	Copies Reqd.	No. of Students	Existing copies	Appx. Price	Amt. (INR)
1	S N Shivanandam, SN Deepa	Principles of Soft Computing (2nd edition)	Wiley India	Req. 32 ✓	92 Rajasthali Hans (Alternate)	60	629	N/R 20128/-
2	K Sam Shanmugam	Digital & Analog Communication System	John Wiley	Req. 60 ✓	92	32	515	31140/-
3	K L P Mishra	Theory of Computer Science: Automata, Lang. & Computation	PHI	Req. 42 ✓	92	50	275	11550/-
4	Galvin	Operating Systems Concepts	Wiley	N/R 00 NIL	92	92 ✓	650	17550/-
5	Tay Vaughan	Multimedia: Making IT work	TMH	Req: 27 ✓	92	65	Not Reqd.	
6		Industrial Sociology		NIL 00 NIL	92	92 ✓		
7		Human Values & Prof. Ethics		NIL 00 NIL	92	92 ✓ Available		

Subject:
1. SC → Rajat
2. Digital & Analog Communication System → Ajit
3. ToC → Anjana
4. OS → Sujata

Teacher (s):

HOD 8/12/15 Dean (Academics) 8KG 9/12/15 Librarian 9/12/15 Director Sir

CENTRAL LIBRARY

BOOKS REQUISITION FORM

Date:

Course: (B.Tech/MBA/MCA/M.Tech) (2015-16)

Branch: ECE

Year/Semester: VI th Sem

To
The Director Sir
IMSECS, Ghaziabad
Respected Sir

It is recommended that the following books may be purchased for the college library. Sanction for purchase may please be accorded. Due to change of Syllabus in VI Sem

S.No.	Author	Title	Publication	Copies Reqd.	No. of Students	Existing copies	Appx. Price (INR)
1.	S M. SZE	VLSI Technology	~~TMH~~ 2nd Edition		113	NIL	650/-

Subject: Integrated Circuit Technology

Teacher (s): 1. Mr. Pankaj Goel
2. Mr. Praveen Kumar
3. Mr. Sajeet Kr

HOD Dean (Academics) Librarian Director Sir

29/12/15

IMS ENGINEERING COLLEGE, GHAZIABAD

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

FACULTY LOAD EVEN SEMESTER (SESSION 2019-20)

Sl.	Faculty Name	Subject Code	Subject	Univ. Load			Total	Actual Load			Total
				L	T	P		L	T	P	
1	Prof. (Dr.) R. P. S. Chauhan (HOD)	KCS403	Microprocessor (CS1)	3	1	0	8	4	2	0	12
		KCS403	Microprocessor (CS2)	3	1	0		4	2	0	
2	Prof. (Dr.) R. N. Baral	REC 085	Wireless & Mobile Communication (EC1)	3	1	0	12	4	2	0	16
		REC 085	Wireless & Mobile Communication (EC2)	3	1	0		4	2	0	
		REC 651	Microwave Engineering Lab (EC2)	0	0	4		0	0	4	
3	Prof. Pankaj Goel (Dean, DSW)	REC 064	Advance Digital Design Using Verilog (EC1)	3	1	0	8	4	2	0	12
		REC 064	Advance Digital Design Using Verilog (EC2)	3	1	0		4	2	0	
4	Prof. (Dr.) Ram Sewak Singh	KEC 401	Communication Engineering	3	0	0	11	5	0	0	15
		KEC 451	Communication Engineering Lab	0	0	4		0	0	4	
		REC 080	Electronics Switching (EC1)	3	1	0		4	2	0	
	Prof. Praveen Kumar	KEC 402	Analog Circuit	3	1	0	11	4	2	0	15
		KEC 452	Analog circuit Lab	0	0	4		0	0	4	
		RIC 603	Control System I (EC2)	3	0	0		5	0	0	
6	Prof. J. N. Vashishtha	KOE 048	Electronics Engineering (CS1)	3	1	0	12	4	2	0	16
		KOE 048	Electronics Engineering (CS2)	3	1	0		4	2	0	
		RIC 651	Microcontrollers for Embeded System Lab (EC2)	0	0	4		0	0	4	
7	Prof. Praveen Chaurasia	REC 601	Microwave Engineering (EC1)	3	1	0	12	4	2	0	16
		REC 601	Microwave Engineering (EC2)	3	1	0		4	2	0	
		RIC 651	Microcontrollers for Embeded System Lab (EC1)	0	0	4		0	0	4	
8	Prof. Balwant Singh	REC 602	Digital Communication (EC1)	3	0	0	14	5	0	0	18
		REC 602	Digital Communication (EC2)	3	0	0		5	0	0	
		REC 652	Communication Lab II (EC1)	0	0	4		0	0	4	
		REC 652	Communication Lab II (EC2)	0	0	4		0	0	4	
9	Prof. Ravi Kumar	ROE082	Entrepreneurship Development (EC1)	3	0	0	10	5	0	0	14
		ROE082	Entrepreneurship Development (EC2)	3	0	0		5	0	0	
		RIC 653	Control System lab I (EC2)	0	0	4		0	0	4	
10	Prof. (Dr.) Neeraj Jain	KEC 403	Signal System	3	1	0	12	4	2	0	16
		KEC 453	Signal System Lab	0	0	4		0	0	4	
		REC 080	Electronics Switching (EC1)	3	1	0		4	2	0	
11	Prof. V. K. Agrawal	KOE 048	Electronics Engineering (CS3)	3	1	0	16	4	2	0	20
		KOE 048	Electronics Engineering (CS4)	3	1	0		4	2	0	
		KCS453	Microprocessor Lab (CS3)	0	0	4		0	0	4	
		KCS453	Microprocessor Lab (CS4)	0	0	4		0	0	4	
12	Prof. Mayurika Saxena	KOE044	Sensor and Instrumentation	3	1	0	12	4	2	0	16
		RIC 653	Control System lab I (EC1)	0	0	4		0	0	4	
		RIC 603	Control System I (EC1)	3	1	0		4	2	0	
13	Prof. Arjun Singh Katiyar	REC065	RADAR Engineering (EC1)	3	1	0	12	4	2	0	16
		REC065	RADAR Engineering (EC2)	3	1	0		4	2	0	
		REC 651	Microwave Engineering Lab (EC1)	0	0	4		0	0	4	
								AVG =			15.54

HoD, ECE

27/12/19

IMS ENGINEERING COLLEGE, GHAZIABAD

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

FACULTY LOAD ODD SEMESTER (SESSION 2018-19)

Sl.	Faculty Name	Subject Code	Subject	University Load			Total	Actual Load			Total
				L	T	P		L	T	P	
1	Prof. Rahul Dayal	REC-051	Antenna and Wave Propagation (EC1) *	3	1	0	8	4	0	0	8
		REC-051	Antenna and Wave Propagation (EC2) *	3	1	0		4	0	0	
2	Prof. Manish Zadoo	ROE-033	Laser Systems and Application (ME1)	3	1	0	14	4	0	0	14
		ROE-033	Laser Systems and Application (ME2)	3	1	0		4	0	0	
		RAS-501	Managerial Economics (CS3)	3	0	0		3	0	0	
		RAS-501	Managerial Economics (2CS)	3	0	0		3	0	0	
3	Prof. R. N. Baral	REC-301	Digital Logic Design (EC2)	3	0	0	9	4	0	0	14
		NOE-072	Quality Management (EC1)-4th Yr	3	0	0		5	0	0	
		NOE-072	Quality Management (2EC)-4th Yr	3	0	0		5	0	0	
4	Prof. Pankaj Goel	NEC-703	VLSI Design (EC1)	3	1	0	14	5	0	0	20
		NEC-703	VLSI Design (EC2)	3	1	0		5	0	0	
		REC-354	Electronics Workshop & PCB Lab (EC1 + EC2)	0	0	4		0	0	8	
		RAS-302	Environment & Ecology (EC1)	2	0	0		2	0	0	
5	Prof. Abhishek Sharma	REC-303	Signals & Systems (EC1)	3	1	0	12	4	4	0	24
		REC-303	Signals & Systems (EC2)	3	1	0		4	4	0	
		REC-353	Signals & Systems Lab (EC1) + (EC2)	0	0	4		0	0	8	
6	Prof. Neeraj Jain	NEC-703	VLSI Design (2EC)	3	1	0	14	5	0	0	19
		RAS-501	Managerial Economics (EC1)	3	0	0		3	0	0	
		RAS-501	Managerial Economics (EC2)	3	0	0		3	0	0	
		NEC-752A	Electronics Circuit Design Lab (EC1 B1 + EC2 B1)	0	0	2		0	0	4	
		NEC-752A	Electronics Circuit Design Lab (2EC)	0	0	2		0	0	4	
7	Prof. J. N. Vashishtha	REC-501	Integrated Circuits (EC2)	3	1	0	12	4	4	0	22
		REC-501	Integrated Circuits (EC1)	3	1	0		4	4	0	
		RAS-302	Environment & Ecology (EC2)	2	0	0		2	0	0	
		REC-551	Integrated Circuits Lab (EC1)	0	0	2		0	0	4	
8	Prof. Praveen Kumar	REC-302	Electronics Devices & Circuits (EC1)	3	1	0	13	4	0	0	18
		REC-302	Electronics Devices & Circuits (EC2)	3	1	0		4	0	0	
		NEC-752A	Electronics Circuit Design Lab (EC2 B2)	0	0	1		0	0	2	
		REC-352	Electronics Devices & Circuits Lab. (EC2)	0	0	2		0	0	4	
		REC-352	Electronics Devices & Circuits Lab. (EC1)	0	0	2		0	0	4	
9	Prof. Sujeet Kumar	REE-305	Network Analysis & Synthesis (EC1)	3	0	0	10	4	4	0	24
		REE-305	Network Analysis & Synthesis (EC2)	3	0	0		4	4	0	
		REC-552	Communication Lab - 1 (EC1)	0	0	2		0	0	4	
		REC-551	Integrated Circuits Lab (EC2)	0	0	2		0	0	4	
10	Prof. Praveen Chaurasia	NEC-032	Digital Image Processing (EC1)	3	1	0	14	5	0	0	16
		NEC-032	Digital Image Processing (EC2)	3	1	0		5	0	0	
		RAS-501	Managerial Economics (CS1)	3	0	0		3	0	0	
		RAS-501	Managerial Economics (CS2)	3	0	0		3	0	0	
11	Prof. Ravi Kumar	NEC-701	Optical Communication (EC1)	3	1	0	13	5	0	0	20
		NEC-032	Digital Image Processing (2EC)	3	1	0		5	0	0	
		NEC-751	Optical Communication & Networking Lab (EC1 B1)	0	0	1		0	0	2	
		REC-554	CAD of Electronics Lab-1 (EC1 + EC2)	0	0	4		0	0	8	
12	Prof. Balwant Singh	REC-503	Digital Signal Processing (EC1)	3	1	0	12	4	4	0	24
		REC-503	Digital Signal Processing (EC2)	3	1	0		4	4	0	
		REC-553	Digital Signal Processing Lab. (EC1)	0	0	2		0	0	4	
		REC-553	Digital Signal Processing Lab. (EC2)	0	0	2		0	0	4	
13	Prof. Jyoti Guglani	REC-301	Digital Logic Design (CS1)	3	0	0	10	5	0	0	18
		REC-301	Digital Logic Design (CS2)	3	0	0		5	0	0	
		REC-351	Digital Logic Design Lab. (CS1)	0	0	2		0	0	4	
		REC-351	Digital Logic Design Lab. (CS2)	0	0	2		0	0	4	
14	Prof. Arjun Singh Katiyar	NEC-701	Optical Communication (EC2)	3	1	0	15	5	0	0	20
		NEC-701	Optical Communication (2EC)	3	1	0		5	0	0	
		REC-051	Antenna and Wave Propagation (EC1) *	3	1	0		4	0	0	
		NEC-751	Optical Comm. & Networking Lab (2EC1 B2)	0	0	1		0	0	2	
		NEC-751	Optical Comm. & Networking Lab (EC1 B2 + EC2 B1)	0	0	2		0	0	4	
15	Prof. Arashdeep Kaur	REC-502	Principles of Communication (EC1)	3	0	0	10	4	4	0	22
		REC-502	Principles of Communication (EC2)	3	0	0		4	4	0	
		RAS-302	Environment & Ecology (IT1 + IT2)	4	0	0		6	0	0	

16	Prof. Pooja Goel	NEC-702B	Data Communication Network (2EC)	3	1	0	14	5	0	0	17
		RAS-502	Sociology (EC1)	3	0	0		2	0	0	
		RAS-502	Sociology (EC2)	3	0	0		2	0	0	
		NEC-752A	Electronics Circuit Design Lab (EC1 B2)	0	0	1		0	0	2	
		NEC-751	Optical Communication & Networking Lab (EC2 B2)	0	0	1		0	0	2	
		REC-552	Communication Lab - 1 (EC2)	0	0	2		0	0	4	
17	Prof. Kamakshi	NEC-702B	Data Communication Networks (EC1)	3	1	0	14	5	0	0	16
		NEC-702B	Data Communication Networks (EC2)	3	1	0		5	0	0	
		REC-051	Antenna and Wave Propagation (EC2) *	3	1	0		4	0	0	
		NEC-751	Optical Communication & Networking Lab (2EC B1)	0	0	2		0	0	2	
18	Prof. V. K. Agarwal	REC-301	Digital Logic Design (CS3)	3	1	0	12	5	0	0	18
		REC-301	Digital Logic Design (2CS)	3	1	0		5	0	0	
		REC-351	Digital Logic Design Lab. (CS3)	0	0	2		0	0	4	
		REC-351	Digital Logic Design Lab. (2CS)	0	0	2		0	0	4	
19	Prof. Ram Sewak Singh	NOE-072	Quality Management (EC2)-4th Yr	3	0	0	10	5	0	0	17
		REC-301	Digital Logic Design (EC1)	3	0	0		4	0	0	
		REC-351	Digital Logic Design Lab. (EC1 + EC2)	0	0	4		0	0	8	
20	Prof. Mayurika Saxena	REC-301	Digital Logic Design (IT1)	3	0	0	10	4	2	0	20
		REC-301	Digital Logic Design (IT2)	3	0	0		4	2	0	
		REC-351	Digital Logic Design Lab. (IT1)	0	0	2		0	0	4	
		REC-351	Digital Logic Design Lab. (IT2)	0	0	2		0	0	4	
21	*Prof. Pravesh Srivastava*	RAS-301	Maths-III (EC1)	3	1	0	8	3	4	0	14
		RAS-301	Maths-III (EC2)	3	1	0		3	4	0	

* REC-051 Allocated to Prof. Arjun Singh and Prof. Kamakshi due to medical condition of Prof. Rahul Dayal.

18.85

09-07-18

1. Faculties Teaching in ECE Department: 16
2. Faculty Teaching in CSE Department: 2
3. Faculty Teaching in IT Department: 1
4. Faculty Teaching in ME Department: 1
5. Faculty Teaching from AS&H Department: 1

IMS ENGINEERING COLLEGE, GHAZIABAD

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

FACULTY LOAD EVEN SEMESTER (SESSION 2018-19)

Sl.	Faculty Name	Subject Code	Subject	University Load			Total	Actual Load			Total
				L	T	P		L	T	P	
1	Prof. Rahul Dayal (HoD)	RAS 601	INDUSTRIAL MANAGEMENT (EC1)	3	0	0	6	3	0	0	6
		RAS 601	INDUSTRIAL MANAGEMENT (EC2)	3	0	0		3	0	0	
2	Prof. Pankaj Goel (Dean, DSW)	REC 405	INTRODUCTION TO MICROPROCESSOR (CSE DEPT)	3	0	0	8	5	0	0	14
		REC 405	INTRODUCTION TO MICROPROCESSOR (CSE DEPT)	3	0	0		5	0	0	
		RIC 651	MICROCONTROLLER AND EMBEDDED SYSTEM LAB	0	0	2		0	0	4	
3	Prof. R.N. Baral	NEC 801	WIRELESS & MOBILE COMMUNICATION	3	1	0	10	5	0	0	11
		RVE 401	UNIVERSAL HUMAN VALUES & PROFESSIONAL ETHICS	3	0	0		3	0	0	
		RVE 401	UNIVERSAL HUMAN VALUES & PROFESSIONAL ETHICS	3	0	0		3	0	0	
4	Prof. Ram Sewak Singh	NEC 802	OPTICAL NETWORK	3	1	0	10	5	0	0	14
		NEC 802	OPTICAL NETWORK	3	1	0		5	0	0	
		REC 453	ELCTRONIC MEASUREMENT & INSTRUMENTATIONS LAB	0	0	2		0	0	4	
5	Prof. Abhishek Sharma	REC 602	DIGITAL COMMUNICATION	3	0	0	9	5	0	0	14
		NEC 802	OPTICAL NETWORK	3	1	0		5	0	0	
		REC 652	COMMUNICATION LAB II	0	0	2		0	0	4	
6	Prof. Jyoti Guglani	REC 401	MICROPROCESSOR & MICROCONTROLLERS	3	0	0	8	5	0	0	14
		REC 401	MICROPROCESSOR & MICROCONTROLLERS	3	0	0		5	0	0	
		REC 451	MICROPROCESSOR & MICROCONTROLLERS LAB	0	0	2		0	0	4	
7	Prof. Praveen Kumar	RIC 603	CONTROL SYSTEM -1	3	0	0	9	5	0	0	14
		NEC 044	ADVANCE DEGITAL DESIGN USING VHDL	3	1	0		5	0	0	
		RIC 653	CONTROL SYSTEM LAB-1	0	0	2		0	0	4	
8	Prof. J.N. Vashishtha	ROE 041	INTRODUCTION TO SOFT COMPUTING	3	1	0	10	4	2	0	16
		ROE 041	INTRODUCTION TO SOFT COMPUTING	3	1	0		4	2	0	
		REC 452	ADVANCE ELECTRONIC SYSTEM LAB	0	0	2		0	0	4	
9	Prof. Sujeet Kumar	REC 064	ADVANCE DIGITAL DESIGN USING VERILOG	3	1	0	10	4	2	0	16
		REC 064	ADVANCE DIGITAL DESIGN USING VERILOG	3	1	0		4	2	0	
		REC 452	ADVANCE ELECTRONIC SYSTEM LAB	0	0	2		0	0	4	
10	Prof. Praveen Chaurasia	REC 402	ELECTROMAGNETIC FIELD THEORY	3	1	0	10	4	2	0	16
		REC 402	ELECTROMAGNETIC FIELD THEORY	3	1	0		4	2	0	
		REC 451	MICROPROCESSOR & MICROCONTROLLERS LAB	0	0	2		0	0	4	
11	Prof. Balwant Singh	NEC 801	WIRELESS & MOBILE COMMUNICATION	3	1	0	9	5	0	0	14
		REC 602	DIGITAL COMMUNICATION	3	0	0		5	0	0	
		REC 652	COMMUNICATION LAB II	0	0	2		0	0	4	
12	Prof. Kamakshi	REC 601	MICROWAVE ENGINEERING	3	0	0	9	4	2	0	15
		NEC 801	WIRELESS & MOBILE COMMUNICATION	3	1	0		5	0	0	
		REC 651	MICROWAVE ENGG LAB	0	0	2		0	0	4	
13	Prof. Ravi Kumar	NEC 044	ADVANCE DEGITAL DESIGN USING VHDL	3	1	0	9	5	0	0	14
		RIC 603	CONTROL SYSTEM -1	3	0	0		5	0	0	
		RIC 653	CONTROL SYSTEM LAB-1	0	0	2		0	0	4	
14	Prof. Neeraj Jain	NEC 044	ADVANCE DEGITAL DESIGN USING VHDL	3	1	0	13	5	0	0	14
		RAS 601	INDUSTRIAL MANAGEMENT (CS2 & CS3)	6	0	0		6	0	0	
		RAS 601	INDUSTRIAL MANAGEMENT (2CS)	3	0	0		3	0	0	
15	Prof. Arjun Singh Katiyar	REC 601	MICROWAVE ENGINEERING	3	1	0	12	4	2	0	16
		REC 651	MICROWAVE ENGG LAB	0	0	2		0	0	4	
		RAS 601	INDUSTRIAL MANAGEMENT (CS1)	3	0	0		3	0	0	
		RUC 601	CYBER SECURITY	3	0	0		3	0	0	
16	Prof. V.K. Agrawal	REC 405	INTRODUCTION TO MICROPROCESSOR (CSE DEPT)	3	0	0	8	5	0	0	14
		REC 405	INTRODUCTION TO MICROPROCESSOR (CSE DEPT)	3	0	0		5	0	0	
		RIC 651	MICROCONTROLLER AND EMBEDDED SYSTEM LAB	0	0	2		0	0	4	
17	Prof. Arashdeep Kaur	REC 403	ELCTRONIC MEASUREMENT & INSTRUMENTATIONS (EC1)	3	0	0	11	4	0	0	15
		REC 403	ELCTRONIC MEASUREMENT & INSTRUMENTATIONS (EC2)	3	0	0		4	0	0	
		REC 453	ELCTRONIC MEASUREMENT & INSTRUMENTATIONS LAB	0	0	2		0	0	4	
		RUC 601	CYBER SECURITY	3	0	0		3	0	0	

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Academic Session 2015-16 (EVEN) , ROOM -303

DAY/TIME	1	2	3	4	5	6	7	8	9	10	11
	08:50-09:50	09:50-10:40	10:40-11:30	11:30-12:20	12:20-01:10	01:10-02:00	02:00-02:50	02:50-03:30	03:30-04:30	04:30-5:30	
MON			NEC 302 2EC	NEC 303 2EC	NEC 304	NAS 301		NEC353(2EC) B1 / NEC-352 PCB B2 (2EC)		NEC 303 2EC	NEC 302 2EC
TUE			NAS 301	NEC 301	NEC 353 (2EC) B2 / NEC 351 (NAS) 2EC B1			NHU 302 2EC	NEC 304	NEC 302 2EC	AUC 002 2EC
WED			NEC 303 2EC	NAS 301	NEC 304	NEC 302 2EC		NEC 301	NAS 301	NEC-352 PCB B1 (2EC) / NEC-354 B2 EDC (2EC)	
THU			NHU 302 2EC	NEC 302 2EC	NEC 351 (NAS) 2EC B2 / NAS 301 B1 T	NEC 304 B1 T		NAS 301	NEC 301	NEC-354 B1 EDC (2EC) / NEC 303 B2 T 2EC	NEC 302 B2 T
FRI			NEC 303 2EC	NEC 301	NEC 302 B1 T / NEC 301 B2 T 2EC	NEC 303 B1 T 2EC / NAS 301 B2 T		NEC 304	NEC 304 B2 / NEC 301 B1 T 2EC	NEC 303 2EC	AUC 002 2EC

Sub. Code	Subject Name	Faculty Name	Lab Code	Lab Name	
NAS-301	Engg. Mathematics-III		NEC-351	Network Analysis & Synthesis Lab	Prof. Sujeet Kumar
NEC-301	Network Analysis & Synthesis	Prof. Sujeet Kumar	NEC-352	Electronics Workshop & PCB Design	Prof. R N baral
NEC-302	Fundamental of Electronic Devices	Prof. Jaya Nidhi Vashishtha	NEC-353	Logic Design Lab.	Prof. Jyoti Gugiani
NEC-303	Signals and Systems	Prof.Abhishek sharma	NEC-354	Electronic Device Lab	Prof. KAMAKSHI
NHU-302	Industrial Sociology	Prof Arjun Singh Katiyar			
NEC-304	Switching Theory & Logic Design	Prof. Jyoti Gugiani			
AUC-002	Cyber Security	Prof. R N baral	Class Cordinator: Prof. Abhishek Sharma		

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CLASS TIME TABLE FOR ECE W.E.F. 02/08/2016

Academic Session 2006-17 (ODD) .

DAY/TIME	1	2	3	4	5	6	7	8	9	10	11
	08:50-09:50	09:50-10:40	10:40-11:30	11:30-12:20	12:20-01:10	01:10-02:00	02:00-02:50	02:50-03:30	03:30-04:30	04:30-5:30	
MON	NAS 301	NEC 353 (LDL) B1		NEC 301	NEC 302		NEC 301 B2 T	NHU 302 EC1	AUC 002		
		NEC-354 B2 EDC					NEC 303 B1 T				
TUE	NEC 302	NEC-304	NEC 353 (LDL) B2		NAS 301		NEC 303	NEC 301	NEC 302		
			NEC-352 PCB B1								
WED	NEC 304	NEC-351 NAS B1		NEC 303	NEC 301		NEC 303	NEC 302	NEC 301 B1 T		
		NEC 302 B2 T	NAS 301 B2 T						NEC 304 B2 T		
THU	NAS 301	NEC 301	NEC 303	NEC-354 B1 EDC			NEC 303	NEC 304	NHU 302 EC1		
				NEC-352 PCB B2							
FRI	NEC 301	NEC 304	NEC 302	NAS 301	NEC 303 B2 T		AUC 002	NEC-351 NAS B2			
					NEC 304 B1 T			NAS 301 B1 T	NEC 302 B1 T		

Sub. Code	Subject Name	Faculty Name	Lab Code	Lab Name	Faculty Name
NAS-301	Engg. Mathematics-III		NEC-351	Network Analysis & Synthesis Lab	Prof. Neeraj Jain
NEC-301	Network Analysis & Synthesis	Prof. Neeraj Jain	NEC-352	Electronics Workshop & PCB Design	Prof. Abhishek Sharma
NEC-302	Fundamental of Electronic Devices	Prof. Praveen Kumar	NEC-353	Logic Design Lab.	Prof Dhaarna Arora
NEC-303	Signals and Systems	Prof. Abhishek Sharma	NEC-354	Electronic Device Lab	Prof. Praveen Kumar
NHU-302	Industrial Sociology	Prof Arjun Singh Katiyar			
NEC-304	Switching Theory & Logic Design	Prof Dhaarna Arora			
AUC-002	Cyber Security	Prof. Kamakshi			

Class Cordinator: Prof. Dhaarna arora

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DAY/TIME	1	2	3	4	5	6	7	8	9	10	11
	08:50-09:50	09:50-10:40	10:40-11:30	11:30-12:20	12:20-01:10	01:10-02:00	02:00-02:50	02:50-03:30	03:30-04:30	04:30-5:30	
MON	NEC 304	NEC 303	NEC 301	AUC 002	NAS 301		NEC 303	NEC-354 B2 EDC			
								NEC-351 NAS B1			
TUE	NEC 353 (LDL) EC2 B2		NEC 304	NHU 302	NEC 302 EC2		NEC 302 B2 T	NAS 301	NEC 301		
	NEC 304 B1 T	NAS 301 B1 T					NEC 303 T B1				
WED	NEC 301	NEC 303	AUC 002	NEC-351 NAS B2			NHU 302	NEC 304	NEC 302 EC2		
				NEC-354 EDC B1							
THU	NEC 302 EC2	NEC 304 B2 T	NEC 303	NAS 301	NEC 304		NEC 302 B1 T	NEC-352 PCB B1			
		NEC 301 B1 T					NEC 303 T B2	NEC 301 B2 T	NAS 301 B2 T		
FRI	NAS 301	NEC 301 EC2	NEC 303	NEC 304	NEC 301		NEC 302 EC2	NEC 353 (LDL) EC2 B1			
								NEC-352 PCB B2			

Sub. Code	Subject Name	Faculty Name	Lab Code	Lab Name	Faculty Name
NAS-301	Engg. Mathematics-III		NEC-351	Network Analysis & Synthesis Lab	Prof. Sujeet Kumar
NEC-301	Network Analysis & Synthesis	Prof. Sujeet Kumar	NEC-352	Electronics Workshop & PCB Design	Prof. R N baral
NEC-302	Fundamental of Electronic Devices	Prof. Praveen Kumar	NEC-353	Logic Design Lab.	Prof. Neeraj Jain(B2)/Prof. Balwant
NEC-303	Signals and Systems	Prof. Balwant Singh	NEC-354	Electronic Device Lab	Prof. Praveen Kumar
NHU-302	Industrial Sociology	Prof. Arjun Singh Katiyar			
NEC-304	Switching Theory & Logic Design	Prof. Jyoti Guglani			
AUC-002	Cyber Security	Prof. R N Baral	Class Cordinator: Prof. Sujeet Kumar		

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	08:50-09:50	09:50-10:40	10:40-11:30	11:30-12:20	12:20-01:10	01:10-02:00	02:00-02:50	02:50-03:40	03:40-04:30	04:30-5:20	5:20:6:10
MON	NEC 703	NEC 702	NOE-071	NEC 031 EC1	NEC 701		NEC 751 OCN				
TUE	NEC 702	NEC 702	NEC 031 EC1	NEC 752 ECD			Project				
WED	NEC 703	NEC 702	NEC 701	NEC 031 EC1	NEC 701						
THU	NEC 703	NEC 701	NOE-071	NEC 031 EC1	NEC 702		NEC 753 Industrial Training Viva Voce				
FRI	NEC 701	NEC 703	NEC 031 EC1	NOE-071	NEC 703						

Subj. Code	Subject Name	Faculty Name
NOE-071	Entrepreneurship Development	Prof. R.N. Baral
NEC 031	Information Theory & Coding	Prof. V K Aggarwal
NEC 701	Optical Communication	Prof. Dhaarna Arora
NEC 702	Data Communication Networks	Prof. Pooja Goel
NEC 703	VLSI Design	Prof. Neeraj Jain

Lab Code	Lab Name	Faculty
NEC 751	Optical Communication & Networking Lab	Prof. Dhaarna Arora
NEC 752	Electronic Circuit Design lab	Prof. R.N. Baral
NEC 753	Industrial Training & Viva Voce	Prof. Pooja Goel
NEC 754	Project	Prof. Neeraj Jain

Class Cordinator: Prof. Neeraj Jain

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Class Time Table: Fourth Year (EC2)

Prepared By: MR

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	08:50-09:50	09:50-10:40	10:40-11:30	11:30-12:20	12:20-01:10	01:10-02:00	02:00-02:50	02:50-03:40	03:40-04:30	04:30-5:20	5:20-6:10
MON	NEC 703	NEC 701	NEC 702	NOE 071	NEC 031 EC2		NEC 702	NEC 703			
TUE	NEC 703	NEC 752 ECD EC2 B1		NEC 031 EC2	NEC 702		NEC 753 Industrial Training Viva Voce				
		NEC 751 OCN EC2 B2									
WED	NOE 071	NEC 752 ECD EC2 B2		NEC 701	NEC 031 EC2		Project				
		NEC 751 OCN EC2 B1									
THU	NEC 701	NEC 703	NOE 071	NEC 702	NEC 031 EC2						
FRI	NEC 703	NEC 701	NEC 701	NEC 031 EC2	NEC 702						

Subj. Code	Subject Name	Faculty Name	Lab Code	Lab Name	Faculty
NOE-071	Entrepreneurship Development	Prof. Pooja Goel	NEC 751	Optical Communication & Networking Lab	Prof. Arjun Singh Katiyar
NEC 031	Information Theory & Coding	Prof. V K Aggarwal	NEC 752	Electronic Circuit Design lab	Prof. R.N. Baral
NEC 701	Optical Communication	Prof. Arjun Singh Katiyar	NEC 753	Industrial Training & Viva Voce	Prof. Kamakshi
NEC 702	Data Communication Networks	Prof. Kamakshi	NEC 754	Project	Prof. Arjun Singh Katiyar
NEC 703	VLSI Design	Prof. Pankaj Goel			

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Class Cordinator: Prof. Arjun Singh Katiyar

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	08:50-09:50	09:50-10:40	10:30-11:30	11:30-12:20	12:20-01:10	01:10-02:00	02:00-02:50	02:50-03:40	03:40-04:30	04:30-5:20	5:20-6:10
MON			NEC 703 2EC	NEC 701	NOE 071 2EC	NEC 702 2EC		NEC 031 2EC	Project		
TUE			NEC 702 2EC	NEC 701	NEC 703 2EC	NEC 031 2EC		NOE 071 2EC	NEC 753 Industrial Training Viva Voce		
WED			NEC 702 2EC	NEC 751 OCN		NEC 701		NEC 031 2EC			
THU			NEC 701	NEC 703 2EC	NEC 703 2EC	NEC 702 2EC		NEC 031 2EC	NEC 701		
FRI			NOE 071 2EC	NEC 702 2EC	NEC 703 2EC	NEC 031 2EC		NEC 752 ECD			

Subj. Code	Subject Name	Faculty Name
NOE-071	Entrepreneurship Development	Prof. Pooja Goel
NEC 031	Information Theory & Coding	Prof. V K Aggarwal
NEC 701	Optical Communication	Prof. Ravi Kumar
NEC 702	Data Communication Networks	Prof. Kamakshi
NEC 703	VLSI Design	Prof. Pankaj Goel

Lab Code	Lab Name	Faculty
NEC 751	Optical Communication & Networking Lab	Ravi Kumar
NEC 752	Electronic Circuit Design lab	Prof. Pooja Goel
NEC 753	Industrial Training & Viva Voce	Prof. Ravi Kumar
NEC 754	Project	Prof. V.K Aggarwal

Class Cordinator: Prof. V.K Aggarwal

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DAY/TIME	1 08:50-09:50	2 09:50-10:40	3 10:40-11:30	4 11:30-12:20	5 12:20-01:10	6 01:10-02:00	7 02:00-02:50	8 02:50-03:30	9 03:30-04:30	10 04:30-5:30	11
MON	NIC 501	NEC 504	PDP EC1	NEC 551 IC EC1 B1 NIC 551 CS B2			NEC 503 EC1	NEC 501	NEC 504		
TUE	NEC 502 EC1	NIC 501	NEC 501	NEC553 MICRO B2 NEC 501 B1 T	NIC 501 EC1 B1 T		NIC 501	NEC 552 COMM. B1 NEC 503 EC1 B	NEC 504 EC1 B2 T		
WED	NEC 502 EC1	NEC 504	NEC 502 EC1	NEC 503 EC1	NHU 501		NEC 501	NEC 502 EC1 B2 T NEC 503 EC1 B1 T	NEC 501		
THU	NEC 502 EC1	NEC 501	NEC 503 EC1	NEC 502 EC1 B1 T NIC 501 EC1 B2 T	NIC 501		NHU 501	NEC 551 IC EC1 B2 NIC 551 CS B1 EC1			
FRI	NIC 501	PDP EC1	NEC 504	NEC 552 COMM. B2 NEC553 MICRO B1			NEC 503 EC1	NEC 502 EC1	NEC 501 EC1 T B2 NEC 504 EC1 B1 T		

Subject Code	Subject Name	Faculty Name
NEC 501	Integrated Circuits	Prof. Manish Zadoo
NEC 502	Principles of Communication	Prof. Arashdeep Kaur
NEC 503	Microprocessors	Prof. Astik Biswas
NIC 501	Control System – I	Prof. Praveen Chaurasia
NEC 504	Antenna and Wave Propagation	Prof. Rahul Dayal
NHU 501	Engineering Economics	Prof. Nitin Aggarwal

Lab Code	Lab Name	Faculty Name
NEC 551	Integrated Circuits Lab	Prof. Manish Zadoo
NIC 551	Control System Lab	Prof. Praveen Chaurasia
NEC 552	Communication Lab – 1	Prof. Arashdeep Kaur
NEC 553	Microprocessors Lab	Prof. Astik Biswas

Class Cordinator: Prof. Arashdeep Kaur

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DAY/TIME	1 08:50-09:50	2 09:50-10:40	3 10:40-11:30	4 11:30-12:20	5 12:20-01:10	6 01:10-02:00	7 02:00-02:50	8 02:50-03:30	9 03:30-04:30	10 04:30-5:30	11
MON	NEC 504	NIC 501	NEC 503	NEC 502	NEC 501		NIC 501	NEC553 MICRO B1			
								NEC 502 B2 T	NEC 504 B2 T		
TUE	NIC 501	NEC 502	NEC 501	NEC 503	NEC 502		NEC 504	NEC 551 IC EC2 B2			
								NEC 501 B1 T	NEC 502 B1 T		
WED	NHU 501	NIC 501 B2 T	NEC 502	NEC553 MICRO B2			NEC 501	NEC 552 COMMU B2			
		NEC 504 B1 T		NIC 551 CS B1				NEC 503 B1 T	NIC 501 B1 T		
THU	NIC 501	PDP	NEC 501	NEC 503	NEC 502		NIC 501	NEC 552 COMMU B1			
								NEC 501 B2 T	NEC 503 B2 T		
FRI	NEC 504	NHU 501	NEC 551 IC EC2 B1		PDP		NEC 501	NEC 504	NEC 503		
			NIC 551 CS B2								

Subject Code	Subject Name	Faculty Name	Lab Code	Lab Name	Faculty Name
NEC 501	Integrated Circuits	Prof. Jaya Nihdi Vashishtha	NEC 551	Integrated Circuits Lab	Prof. Manish Zadoo
NEC 502	Principles of Communication	Prof. Balwant Singh	NIC 551	Control System Lab	Prof. Ravi Kumar(B2) / Prof. Pooja Goel(B1)
NEC 503	Microprocessors	Prof. RPS Chauhan	NEC 552	Communication Lab – 1	Prof. Balwant Singh
NIC 501	Control System – I	Prof. Praveen Chaurasia	NEC 553	Microprocessors Lab	Prof. RPS Chauhan
NEC 504	Antenna and Wave Propagation	Prof. Manish Zadoo			
NHU 501	Engineering Economics	Prof. Jyoti Guglani	Class Cordinator: Prof. Manish Zadoo		

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	08:50-09:50	09:50-10:40	10:30-11:30	11:30-12:20	12:20-01:10	01:10-02:00	02:00-02:50	02:50-03:40	03:40-04:30	04:30-5:20	5:20-6:10
MON			NEC 502 2EC	NEC 503 2EC	NEC 504 2EC	NEC 502 2EC		NEC 552 COMM		NEC 501 2EC	NIC 501
TUE			NIC 501	NEC 501 2EC	NEC 502 2EC	NEC 504 2EC		NHU 501	PDP	NEC 503 2EC T	NEC 501 2EC T
WED			NEC 501 2EC	NEC 504 2EC	NEC 503 2EC	PDP		NEC 551 IC 2EC		NEC 503 2EC	NIC 501 T
THU			NEC 504 2EC	NEC 503 2EC	NIC 501	NEC 502 2EC		NEC 503 2EC	NEC 502 2EC	NIC 551 CS 2EC	
FRI			NEC 502 2EC	NEC 501 2EC	NIC 501	NIC 501		NEC 504 2EC T	NHU 501	NEC 553 MICRO	

Sub. Code	Subject Name	Faculty Name
NEC 501	Integrated Circuits	Prof. Jaya Nidhi Vashishtha
NEC 502	Principles of Communication	Prof. Arashdeep Kaur
NEC 503	Microprocessors	Prof Astik Biswas
NIC 501	Control System – I	Prof. Ravi kumar
NEC 504	Antenna and Wave Propagation	Prof. Rahul Dayal
NHU 501	Engineering Economics	Prof. Praveen Chaurasia

Lab Code	Lab Name	Faculty Name
NEC 551	Integrated Circuits Lab	Prof. Pankaj Goel
NIC 551	Control System Lab	Prof. Ravi Kumar
NEC 552	Communication Lab – 1	Prof. Arashdeep Kaur
NEC 553	Microprocessors Lab	Prof Astik Biswas

Class Cordinator: Prof. Astik Biswas

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Prepared by:	Approved by: Director

CLASS TT EC1 2ND YEAR

Academic Session2016-17(EVEN)

ROOM NO-C 301

DAY/TIME	Period-1	Period-2	Period-3	Period-4	Period-5	Period-6	Period-7	Period-8	Period-9	TUTE B1	C 301
	8:50-9:50	9:50-10:40	10:40-11:30	11:30-12:20	12:20-1:10 PM	1:10-2:00	2:00-2:50	2:50-3:40	3:40-4:30	TUTE B2	C-309
MON	NEC 404	NOE 043	NEC 403	NEC 401(EC1)	NHU 401		DS LAB Lab 5 EC1 B1		NEC 402T B1		
							NEC 452 B2		NEC404 T B2		
TUE	NEC 403	NEC 402	DS LAB Lab 5 EC1 B2		AUC 001		NOE 043	NEC 402	NHU 401		
			NEC 452 B1								
WED	NEC 401(EC1)	NEC 402	NOE 043	NEC 454 EC1 B2			NEC 404	NEC404 T	NEC 403		
				NEC 453 EC1 B1				NEC 401T			
THU	NEC 404	NEC 404	NEC 402	AUC 001	NEC 403		NEC 403T B2	NEC 401(EC1)	NOE 043		
							NEC 401T B1				
FRI	NEC 402	NEC 404	NEC 403	NHU 401	NEC 402T B2		NEC 401(EC1)	NEC 454 EC1 B1			
					NEC 403T B1			NEC 453 EC1 B2			
SAT											

CODE	SUBJECT	FACULTY	CODE	LAB	FACULTY	ROOM
NOE 042	NANO SCIENCE	Prof. Pradeep Kumar	NEC 451	Data structure lab	Prof. Vishan Gupta	C BLOCK LAB 5
NEC 401	DATA STRUCTURE	Prof. Vishan Gupta	NEC 452	Electronic Circuits Lab	Prof. Ravi kumar	C BLOCK EC LAB 1
NEC 402	ELECTRONIC CIRCUIT	Prof. Praveen kumar	NEC 453	Digital Electronics Lab	Prof. Dhaarna Arora	C BLOCK EC LAB 3
NEC 403	EMI	Prof. Arashdeep kaur	NEC 454	EMI Lab	Prof. Arashdeep kaur	C BLOCKEN LAB
NEC 404	EMFT	Prof. Praveen Chaurasiya				
NHU 401	INDUSTRIAL PSCHYCOLOGY	Prof. Ravi Kumar				
AUC 001	HUMAN VALUES	Dr. Suman Gupta				

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CLASS TT EC2 2ND YEAR

Academic Session2016-17(EVEN)

ROOM NO-C 302

DAY/TIME	Period-1	Period-2	Period-3	Period-4	Period-5	Period-6	Period-7	Period-8	Period-9	TUTE B1	C 302
	8:50-9:50	9:50-10:40	10:40-11:30	11:30-12:20	12:20-1:10 PM	1:10-2:00	2:00-2:50	2:50-3:40	3:40-4:30	TUTE B2	C-310
MON	NEC 402 EC2	NEC 404	NEC 401	NEC 452 EC2 B1 / NEC 454 EC2 B2			NHU 401	NEC 403 EC2	NEC 404		
TUE	NEC 402 EC2	NOE 043	AUC 001	NEC 403 EC2	NEC 404		NEC 404 T B1 / NEC 401T EC2 B2	DS LAB Lab 5 EC2 B1 / NEC 453 EC2 B2			
WED	NEC 403 EC2	NOE 043	NEC 402 EC2	NEC 404	NEC 401		NEC 402T EC2 B1 / NEC 404T EC2 B2	DS LAB Lab 5 EC2 B2 / NEC 453 EC2 B1			
THU	NEC 402 EC2	NEC 403 EC2	NEC 401	NEC 452 EC2 B2 / NEC 454 EC2 B1			NEC 402T EC2 B2 / NEC 401 T B1	NOE 043	NEC 403 EC2		
FRI	NEC 403 EC2	NOE 043	NEC 404	AUC 001	NEC 401		NHU 401	NEC 402 EC2	NHU 401		
SAT											

CODE	SUBJECT	FACULTY
NOE 042	NANO SCIENCE	Prof. Pradeep Kumar
NEC 401	DATA STRUCTURE	Prof. Promod Nath
NEC 402	ELECTRONIC CIRCUIT	Prof. Praveen kumar
NEC 403	EMI	Prof. Arashdeep kaur
NEC 404	EMFT	Prof. Arjun Singh Katiyar
NHU 401	INDUSTRIAL PSCHYCOLOGY	Prof. Ravi Kumar
AUC 001	HUMAN VALUES	Dr. Suman Gupta

CODE	LAB	FACULTY	ROOM
NEC 451	Data structure lab	Prof.	C BLOCK LAB 5
NEC 452	Electronic Circuits Lab	Prof. Praveen kumar	C BLOCK EC LAB 1
NEC 453	Digital Electronics Lab	Prof. Balwant Singh	C BLOCK EC LAB 3
NEC 454	EMI Lab	Prof. Balwant singh	C BLOCKEN LAB

IMS ENGINEERING COLLEGE	IMSEC/QF/08b
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	Issue No: 01
Faculty Time Table	Issue Date: 1 May 2010
Prepared by:	Approved by: Director

CLASS TT 2EC 2ND YEAR

Academic Session2016-17(EVEN) — **ROOM NO-C 303**

DAY/TIME	Period-1	Period-2	Period-3	Period-4	Period-5	Period-6	Period-7	Period-8	Period-9	Period-10	Period-11
	8:50-9:50	9:40-10:40	10:40-11:30	11:30-12:20	12:20-1:10 PM	1:10-2:00	2:00-2:50	2:50-3:40	3:40-4:30	4:30 - 5:20	5:20 - 6:10
MON			AUC 001	NEC 401	NEC 404 2EC	NOE 043 2EC		NEC 401 T B1 NEC 404 T B2	NEC 452 2EC B2 DS LAB Lab 5 2EC B1		NEC 403T B2 NEC402T B1
TUE			NEC 402	NHU 401	NEC 454 2EC B2 NEC 453 2EC B1			NOE 043 2EC	NEC 404 2EC	NEC 402	NEC 401
WED			NEC 403	NEC 401	NEC 404 2EC	NEC 402		AUC 001	NOE 043 2EC	NEC 403T B1 NEC402T B2	NEC 403
THU			NEC 403	NEC 401	NEC 404 2EC	NEC 404 2EC		NEC 401 T B2 2 NEC 404 T B1	NHU 401	NEC 403	NEC 402
FRI			NEC 402	NOE 043 2EC	NEC 454 2EC B1 NEC 453 2EC B2			NHU 401	DS LAB Lab 5 2EC B2 NEC 452 2EC B1		NEC 403
SAT											

CODE	SUBJECT	FACULTY	CODE	LAB	FACULTY	ROOM
NOE 043	Laser Systems and Applications	Prof. Pradeep Kumar	NEC 451	Data structure lab	Prof.	C BLOCK LAB 5 C BLOCK EC LAB 1
NEC 401	DATA STRUCTURE	Prof. Promod Nath	NEC 452	Electronic Circuits Lab	Prof. J. N. Vashishtha	C BLOCK EC
NEC 402	ELECTRONIC CIRCUIT	Prof. J. N. Vashishtha	NEC 453	Digital Electronics Lab	Prof. Dhaarna Arora	C BLOCKEN LAB
NEC 403	EMI	Prof. Ravi Kumar	NEC 454	EMI Lab	Prof. Vivek Chaudhary	EN LAB
NEC 404	EMFT	Prof. Praveen Chaurasiya				
NHU 401	INDUSTRIAL PSCHYCOLOGY	Prof. Neeraj Jain	TUTE B1	C 303		
AUC 001	HUMAN VALUES	Dr. Suman Gupta	TUTE B2	C-311		

IMS ENGINEERING COLLEGE	IMSEC/QF/08b
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	Issue No: 01
Faculty Time Table	Issue Date: 1 May 2010
Prepared by:	Approved by: Director

CLASS TT EC1 3RD YEAR

Academic Session2016-17(EVEN) — ROOM NO-C 304

DAY/TIME	Period-1	Period-2	Period-3	Period-4	Period-5	Period-6	Period-7	Period-8	Period-9	TUTE B1	C 304
	8:50-9:50	9:50-10:40	10:40-11:30	11:30-12:20	12:20-1:10 PM	1:10-2:00	2:00-2:50	2:50-3:40	3:40-4:30	TUTE B2	C-309
MON	NEC 603	NEC 014	NEC 601 EC1	NEC 602 EC1	NIC 601R		NHU 601	NEC 651 R EC1 B1 / NEC 652 EC1 B2			
TUE	NEC 014	NIC 601R	NIC 601R	NEC 601 EC1	NEC 602 EC1		NEC 603	NEC 601 T B1 / NEC 602 T B2	NHU 601		
WED	NEC 014	NIC 601R	NEC 653 EC1 B2 / NEC 651 EC1 B1		NEC 602 EC1		NEC 602 EC1	NEC 603	NEC 601 EC1		
THU	NHU 601	NEC 014	NIC 601R	NEC 653 EC1 B1 / NEC 651 EC1 B2			NEC 603	NEC 601 EC1	NEC 014		
FRI	NEC 014	NEC 603	NEC 651 R EC1 B2 / NEC 652 EC1 B1		NEC 601 EC1		NEC 601 T B2 / NEC 602 T B1	NIC 601R	NEC 602 EC1		
SAT											

CODE	SUBJECT	FACULTY	CODE	LAB	FACULTY	ROOM
NEC 601	Microwave Engineering	Prof. Kamakshi	NEC 651	Antenna and Microwave Lab	Prof. Kamakshi	C BLOCK EC LAB 2
NEC 602	Digital Communication	Prof. Abhishek sharma	NEC 652	Communication Lab – II	Prof. Abhishek sharma	C BLOCK EC LAB 4
NEC 603	Integrated CircuitTechnology	Prof. Neeraj Jain	NEC 653	CAD of Electronics Lab	Prof. Neeraj Jain	C BLOCK LAB 5
NEC 014	Advance Semiconductor Devices	Prof. Jyoti guglani	NIC 651R	Microcontroller for Embedded System Lab	Prof. Jyoti guglani	B BLOCK EC
NIC 601R	Microcontroller for Embedded System	Prof. R.P.S. Chauhan				
NHU 601	Industrial Management	Prof. Pooja Goel				

HOD ECE

IMS ENGINEERING COLLEGE	IMSEC/QF/08b
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	Issue No: 01
Faculty Time Table	Issue Date: 1 May 2010
Prepared by:	Approved by: Director

CLASS TT EC2 3RD YEAR

Academic Session2016-17(EVEN)

ROOM NO-C 305

DAY/TIME	Period-1	Period-2	Period-3	Period-4	Period-5	Period-6	Period-7	Period-8	Period-9	TUTE B1	C 305
	8:50-9:50	9:50-10:40	10:40-11:30	11:30-12:20	12:20-1:10 PM	1:10-2:00	2:00-2:50	2:50-3:40	3:40-4:30	TUTE B2	C-310
MON	NEC 014 EC2	NEC 602	NIC 601R EC2	NIC 601R EC2	NEC 603		NHU 601	NEC 601	NEC 603		
TUE	NEC 651R EC2 B1 / NEC 652 EC2 B2		NEC 601	NIC 601R EC2	NEC 603		NHU 601	NEC 602	NEC 014 EC2		
WED	NEC 602	NEC 014 EC2	NIC 601R EC2	NEC 601	NEC 603		NEC 602	NEC 651R EC2 B2 / NEC 652 EC2 B1			
THU	NEC 014 EC2	NEC 601	NEC 603	NIC 601R EC2	NHU 601		NEC 653 EC2B1 / NEC 651 EC2 B2		NEC 602		
FRI	NEC 602	NEC 601	NIC 601R EC2	NEC 603	NEC014		NEC 653 EC2 B2 / NEC 651 EC2 B1		NEC 601		
SAT											

CODE	SUBJECT	FACULTY	CODE	LAB	FACULTY	ROOM
NEC 601	Microwave Engineering	Prof. Rahul Dayal	NEC 651	Antenna and Microwave Lab	Prof. Arjun Singh kKatiyar	C BLOCK EC LAB 2
NEC 602	Digital Communication	Prof. Pooja Goel	NEC 652	Communication Lab – II	Prof. Pooja Goel	C BLOCK EC LAB 4
NEC 603	Integrated CircuitTechnology	Prof. Sujeet Kumar	NEC 653	CAD of Electronics Lab	Prof. Sujeet Kumar	C BLOCK LAB 5
NEC 014	Advance Semiconductor Devices	Prof. Jyoti Guglani	NIC 651R	Microcontroller for Embedded System Lab	Prof. pankaj Goel/Prof. Jyoti guglani	B BLOCK EC
NIC 601R	Microcontroller for Embedded System	Prof. R. P. S. Chauhan				
NHU 601	Industrial Management	Prof. R. N. Baral				

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CLASS TT 2EC 3RD YEAR

Academic Session2016-17(EVEN) — ROOM NO-C 306

DAY/TIME	Period-1	Period-2	Period-3	Period-4	Period-5	Period-6	Period-7	Period-8	Period-9	Period-10	Period-11
	8:50-9:50	9:50-10:40	10:40-11:30	11:30-12:20	12:20-1:10 PM	1:10-2:00	2:00-2:50	2:50-3:40	3:40-4:30	4:30 - 5:20	5:20 - 6:10
MON			NEC 014	NEC 601	NEC 014	NIC 601R		NEC 601	NEC 651		NEC 602 2EC
TUE			NEC 603 2EC	NEC 603 2EC	NIC 601R	NEC 602 2EC		NEC 014	NHU601 2EC	NEC 602 2EC	NEC 601
WED			NEC 014	NEC 602 2EC	NIC 601R	NEC 601		NIC 601R	NEC 014	NEC 603 2EC	NHU601 2EC
THU			NEC 652 2EC		NEC 602 2EC	NEC 014		NIC 601R	NEC 653 2EC		NEC 603 2EC
FRI			NEC 603 2EC	NEC 601	NIC 651R			NIC 601R	NHU601 2EC	NEC 601	NEC 602 2EC
SAT											

CODE	SUBJECT	FACULTY	CODE	LAB	FACULTY	ROOM
NEC 601	Microwave Engineering	Prof. Kamakshi	NEC 651	Antenna and Microwave Lab	Prof. R. N. Baral	C BLOCK EC LAB 2
NEC 602	Digital Communication	Prof. Abhishek sharma	NEC 652	Communication Lab – II	Prof. Abhishek sharma	C BLOCK EC LAB 4
NEC 603	Integrated CircuitTechnology	Prof. Sujeet kumar	NEC 653	CAD of Electronics Lab	Prof. J. N. Vashishtha	C BLOCK LAB 5
NEC 014	Advance Semiconductor Devices	Prof. J. N. Vashishtha	NIC 651R	Microcontroller for Embedded System Lab	Prof. Pankaj Goel	B BLOCK EC
NIC 601R	Microcontroller for Embedded System	Prof. Pankaj Goel		TUTE B1 C 306		
NHU 601	Industrial Management	Prof. R. N. Baral		TUTE B2 C-311		

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CLASS TT EC1 4TH YEAR

Academic Session2016-17(EVEN)

DAY/TIME	Period-1	Period-2	Period-3	Period-4	Period-5	Period-6	Period-7	Period-8	Period-9
	8:50-9:50	9:50-10:40	10:40-11:30	11:30-12:20	12:20-1:10 PM	1:10-2:00	2:00-2:50	2:50-3:40	3:40-4:30
MON	NEC 801 EC1	NOE 081	NEC 041 EC1	NEC 041 EC1	NEC 802 EC1				
TUE	NEC 802 EC1	NEC 801 EC1	NEC 802 EC1	NOE 081	NEC 801 EC1				
WED	NOE 081	NEC 041 EC1	NEC 801 EC1	NOE 081	NEC 802 EC1				
THU	NEC 801 EC1	NEC 041 EC1	NOE 081	NEC 041 EC1	NEC 802 EC1				
FRI	NEC 041 EC1	NOE 081	NEC 801 EC1	NEC 802 EC1					
SAT									

CODE	SUBJECT	FACULTY
NEC 081	NCER	Prof. Pankaj Goel
NEC 802	OPTICAL NETWORK	PROF Manish Zadoo
NEC 041	ELECTRONIC SWITCHING	Prof. Dhaarna Arora
NEC 801	IRELESS & MOBILE COMMU	Prof. Balwant Singh

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IMS ENGINEERING COLLEGE	IMSEC/QF/08b
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Faculty Time Table	Issue Date: 1 May 2010
Prepared by:	Approved by: Director

CLASS TT EC2 4TH YEAR

Academic Session2016-17(EVEN)

DAY/TIME	Period-1	Period-2	Period-3	Period-4	Period-5	Period-6	Period-7	Period-8	Period-9
	8:50-9:50	9:50-10:40	10:40-11:30	11:30-12:20	12:20-1:10 PM	1:10-2:00	2:00-2:50	2:50-3:40	3:40-4:30
MON	NEC 041EC2	NEC 802 EC2	NEC 801 EC2	NOE 081	NOE 081				
TUE	NEC 801 EC2	NEC 041EC2	NEC 041EC2	NOE 081	NEC 802 EC2				
WED	NEC 041 EC2	NEC 802 EC2	NEC 802 EC2	NEC 801 EC2	NOE 081				
THU	NEC 802 EC2	NEC 801 EC2	NOE 081	NOE 081	NEC 041EC2				
FRI	NEC 801 EC2	NEC 041EC2	NEC 802 EC2	NEC 801 EC2					
SAT									

CODE	SUBJECT	FACULTY
NEC 081	NCER	Prof. Arjun Singh Katiyar
NEC 802	OPTICAL NETWORK	PROF Manish Zadoo
NEC 041	ELECTRONIC SWITCHING	Prof. Dhaarna Arora
NEC 801	IRELESS & MOBILE COMMU	Prof. Balwant Singh

CODE	LAB	FACULTY

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Faculty Time Table	Issue Date: 1 May 2010
Prepared by:	Approved by: Director

CLASS TT 2EC 4TH YEAR

Academic Session2016-17(EVEN)

DAY/TIME	Period-1	Period-2	Period-3	Period-4	Period-5	Period-6	Period-7	Period-8	Period-9
	8:50-9:50	9:50-10:40	10:40-11:30	11:30-12:20	12:20-1:10 PM	1:10-2:00	2:00-2:50	2:50-3:40	3:40-4:30
MON		NEC 802 2EC	NEC 801	NEC 081 2EC	NEC 802 2EC	NEC 041 2EC			
TUE		NEC 041 2EC	NEC 801	NEC 802 2EC	NEC 041 2EC	NEC 081 2EC			
WED		NEC 041 2EC	NEC 802 2EC	NEC 801	NEC 801	NEC 081 2EC			
THU		NEC 041 2EC	NEC 081 2EC	NEC 801	NEC 802 2EC	NEC 081 2EC			
FRI			NEC 801	NEC 802 2EC	NEC 041 2EC	NEC 081 2EC			
SAT									

CODE	SUBJECT	FACULTY	CODE	LAB	FACULTY
NEC 081	NCER	PROF Manish Zadoo			
NEC 802	OPTICAL NETWORK	Prof. Rahul Dayal			
NEC 041	ELECTRONIC SWITCHING	Prof. Neeraj Jain			
NEC 801	WIRELESS & MOBILE COMMU	Prof. RN Baral			

IMSEC
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LESSON PLAN

Department :	Electronics & Communication Engineering
Subject & Code :	VLSI Design (REC-702)
Name of Faculty :	Pankaj Goel
Text Book :	T1: Neil H.E. Weste, David M. Harris, "cmos VLSI Design" – A ckt & System Perspective", Pearson, 4th edition
	T2: Sung-mo Kang & Yusuf Leblebici, "Cmos digital IC : Analysis & Design", 3rd edition, by TMH, 4th edition

Lecture No.	Unit	Topics to be covered
1	1	Introduction to VLSI Design, History, Preview
2	1	VLSI Design flow – ASIC & FPGA
3	1	MOSFET Working, Types of MOSFETs
4	1	cmos Logic – Introduction
5	1	cmos logic gates impl. – Combinational ckts
6	1	" " " " – " "
7	1	" " " " – Sequential ckts
8	1	" " " " – " "
9	1	" " " " – using Pass Transistors
10	1	cmos fabrication Process using N-well
11	1	" " " " "
12	1	Layout design rules, layout of cmos Inverter
13	1	cmos layout of 2-input NAND, NOR gates
14	1	" " of 3-input NAND gate
15	1	Stick diagram
16	1	Design Partitioning, Y-chart
17	1	logic design, ckt design, Physical design
18	1	Design verification, fabrication, Packaging & Testing
19	2	Delay – Introduction, Propagation delay, Contamination delay
20	2	Transient response
21	2	RC delay model – Introduction, Inverter model
22	2	Analysis of 2-input logic gates (NAND) using RC model
23	2	" " 3-input NAND gate using RC delay"
24	2	Linear delay model
25	2	" " "
26	2	Logical effort of Pathe

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Odd/Even Sem.(Session - 2020-21)

LESSON PLAN

Year : 4th	Semester : 7th	Section : EC1
Reference Books	R1 : D.A. Pucknell and K. Eshraghian, "Basic VLSI Design: Systems and circuits", PHI, 3rd edition 1994	
	R2:	
	R3: W. Wolf, "Modern VLSI Design: System on chip", 3rd edition, Pearson 2003	

Text Book/Ref. Book Page No./e-Sources	Date of Lecture Scheduled	Date of Lecture Held	Remarks
(Neil H. Weste) Text Book T1 Page nos 1-6	10-08-20	10-08-20	
(Kang) Text Book T2 Page nos 21-23	14-08-20	14-08-20	
Text Book T1 Page nos 6-8	17-08-20	17-08-20	
T1 Page nos 9-10	19-08-20	19-08-20	
T1 Page nos 11-12	21-08-20	21-08-20	
"	24-08-20	24-08-20	
T1 Page nos 18-19	26-08-20	26-08-20	
T1 Page nos 16-19	28-08-20	28-08-20	
T1 Page nos 13-15	31-08-20	31-08-20	
T1 Page nos 19-21	02-09-20	02-09-20	
T1 Page nos 22-24	07-09-20	07-09-20	
T1 Page nos 24-25	09-09-20	09-09-20	
T1 Page nos 26-27	11-09-20	11-09-20	
T1 Page nos 27-28	14-09-20	14-09-20	
T1 Page nos 28-29	15-09-20	15-09-20	
T1 Page nos 29-31	16-09-20	16-09-20	
T1 Page nos 32-45	18-09-20	18-09-20	
T1 Page nos 53-55	21-09-20	21-09-20	
T1 Page nos 141-142	23-09-20	23-09-20	
T1 Page nos 143-145	25-09-20	25-09-20	
T1 Page nos 146-147	28-09-20	28-09-20	
T1 Page nos 148, 151	30-09-20	30-09-20	
T1 Page nos 155-158	05-10-20	05-10-20	
T1 Page nos 159-163	07-10-20	07-10-20	
T1 Page nos 163-164	09-10-20	09-10-20	

Signature of Subject Teacher

Signature of HOD

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GHAZIABAD

LESSON PLAN

Department :	Electronics & Communication Engineering
Subject & Code :	VLSI Design (REC-702)
Name of Faculty :	Pankaj Goel
Text Book :	T1:
	T2:

Lecture No.	Unit	Topics to be covered
1	2	logical effort of Pathe → Examples
2	2	Timing Analysis Delay models
3	2	Power - Introduction
4	2	Components of Dynamic Power dissipation
5	2	Techniques to reduce " "
6	2	Components of Static " "
7	2	Techniques to reduce " " " - Multiple Threshold Voltage, ~~Scaling~~ VT cmos
8	2	" " " " " " - Power Gating, Threshold Voltage
9	3	Energy-delay optimization
10	3	Low Power Architectures
11	3	Interconnect : Introduction
12	3	" modelling
13	3	" Impact
14	3	" Engineering - Techniques for resistance
15	3	" " - Techniques " Capacitance
16	3	Logical effort with wires
17	5	Design for Testability - Introduction
18	5	Controllability, observability, fault types & models
19	5	Scan based technique
20	5	" " "
21	5	BIST technique, LFSR
22	5	Low-Power CMOS - Introduction
23	5	overview of Power Consumption, Power design through
24	5	voltage Scaling, Switching Activity, Switched Capacitance
25	5	Adiabatic Logic
26	4	Dynamic logic Ckts - Basic Principle of Pass Tr

Odd/Even Sem.(Session - 2020-21)

LESSON PLAN

Year : 4th		Semester : 7th	Section : EC1
Reference Books	R1 :		
	R2:		
	R3:		

Text Book/Ref. Book Page No./e-Sources	Date of Lecture		Remarks
	Scheduled	Held	
Text Book T1 Page nos 165-167	12-10-20	12-10-20	
T1 Page nos 171, 173-174	14-10-20	14-10-20	
T1 Page nos 181-182	16-10-20	16-10-20	
T1 Page nos 184-185	21-10-20	21-10-20	
T1 Page nos 186-188, 189-193	26-10-20	26-10-20	
T1 Page nos 194-197	28-10-20	28-10-20	
T1 Page nos 199-200	30-10-20	30-10-20	
T1 Page nos 197-198	02-11-20	02-11-20	
T1 Page nos 200-204	04-11-20	04-11-20	
T1 Page nos 204-206	06-11-20	06-11-20	
T1 Page nos 211-212	09-11-20	09-11-20	
T1 Page nos 213-218	11-11-20	11-11-20	
T1 Page nos 220-224	18-11-20	18-11-20	
T1 Page nos 229-232	20-11-20	20-11-20	
T1 Page nos 232-234	09-12-20	09-12-20	
T1 Page nos 236-238	10-12-20	10-12-20	
(Kaing) Text Book T2 Page nos 622-623	11-12-20	11-12-20	
T2 Page nos 624-628	14-12-20	14-12-20	
T2 Page nos 630-632	16-12-20	16-12-20	
T2 Page nos 632-634	17-12-20	17-12-20	
T2 Page nos 481-482	18-12-20	18-12-20	
T2 Page nos 483-490	30-12-20	30-12-20	
T2 Page nos 491-495, 498-504, 508	31-12-20	31-12-20	
T2 Page nos 512-514	01-01-21	01-01-21	
T2 Page nos 357-358, 359-61	04-01-21	04-01-21	

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LESSON PLAN

Department :	Electronics & Communication Engineering
Subject & Code :	VLSI Design (REC-702)
Name of Faculty :	Pankaj Goel
Text Book :	T1:
	T2:

Lecture No.	Unit	Topics to be covered
1	4	Synchronous dynamic ckt techniques
2	4	dynamic cmos " "
3	4	Domino cmos " "
4	4	Semiconductor memories - introduction
5	4	Dyamic RAM
6	4	Static "
7	4	Rom, Flash memory
8		
9		
10		
11		
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13		
14		
15		
16		
17		
18		
19		
20		
21		
22		
23		
24		
25		
26		

Odd/Even Sem.(Session - 2020-21)

LESSON PLAN

Year : 4th		Semester : 7th	Section : EC1
Reference Books	R1 :		
	R2:		
	R3:		

Text Book/Ref. Book Page No./e-Sources	Date of Lecture Scheduled	Date of Lecture Held	Remarks
T2 Page nos 374-378	06-01-2021	07-01-21 08-01-21	
T2 Page nos 379-380	07-01-2021	11-01-21	
T2 Page nos 381-383	08-01-2021	13-01-21	
T2 Page nos 405-407	11-01-2021	14-01-21	
T2 Page nos 410-425	13-01-2021	15-01-21	
T2 Page nos 438-450	14-01-2021	18-01-21	
T2 Page nos 451-470	15-01-2021	20-01-21	

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COURSE FILE

OF

Integrated Circuits

(KEC 501)

2020-2021

DEPARTMENT OF
ELECTRONICS & COMMUNICATION
ENGINEERING

IMS ENGINEERING COLLEGE, GHAZIABAD

Faculty Name: Praveen Kumar

Branch: Electronics and Communication *Engineering*

Semester: 5th

Session: 2020-21

Subject Name: Integrated Circuits

Subject Code: KEC 501

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Prepared by: MR	Approved by: Director

	Particulars
1.	Quality Policy (on left inside cover of Course File)
2.	Institute Mission and Vision
3.	Departmental Mission and Vision
5.	Program Outcomes (PO)
6.	Program Educational Objectives (PEO) and Program Specific Outcomes (PSO)
7.	Academic Calendar
8	Time Table
9	Student List
10.	University Evaluation Scheme
11.	Syllabus (Theory)
12.	Course Outcome, Mapping with PO/PSO
13.	Syllabus (Practical) with Experiment List mapped with Course Outcomes
14.	Topics beyond Syllabus
15.	Quiz/Assignment/Tutorial Records
16.	CT Question Paper (mapped with CO)
17.	Sessional Marks Analysis
18.	Lecture Notes/PPT
19.	Question Bank
20	Last three years University Question Paper (AKTU) with Solution
21	Attendance Register

Name and Signature of Course Instructor	Signature of HoD
Pravesh Kr	
	Space for Internal Auditor's Use

IMSEC, GHAZIABAD

Department of Electronics and Communication Engineering

Vision of the Institution

Our vision is to impart vibrant, innovative and global education to make IMS the world leader in terms of excellence of education, research and to serve the nation in the 21st century.

Mission of the Institution:

- To develop IMSEC as a centre of Excellence in Technical and Management education.
- To inculcate in its students the qualities of Leadership, Professionalism, Executive competence and corporate understanding.
- To imbibe and enhance Human Values, Ethics and Morals in our students.
- To transform students into Globally Competitive professionals.

Vision (Department):

To produce highly competent engineers by imparting innovative and accomplished information through global education and adequately prepare them to face the challenges of outside world by fulfilling the requirements of Electronics & Communication industries.

Mission (Department):

- To make the department a centre of excellence in Electronics & Communication Engineering and to produce eminent engineers.
- To inculcate professionalism, team work, leadership qualities by imbibing high human values and professional ethics, in students.
- To enhance the employability of students by giving inter-disciplinary knowledge to meet the need of society and become globally competitive professionals.
- To become a centre for research in the stream of Electronics & Communication Engineering and to provide excellent learning environment for researchers by promoting research activities in the department.

IMSEC, GHAZIABAD

Department of Electronics and Communication Engineering

PROGRAM OUTCOMES (POs)

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization for the solution of complex engineering problems.
2. **Problems analysis:** Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design development and solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for public health and safety and cultural, societal and environmental considerations.
4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources and modern engineering IT tools, including prediction and limitations.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts and demonstrate the knowledge of and need for sustainable development.
8. **Ethics:** Apply ethical principles, commit to professional ethics, responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual, as a member or leader in diverse teams and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with the society at large. To be able to comprehend and write effective reports, design documentation, make presentations, give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge, understanding of the engineering and management principles. Apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for and have the preparation, ability to engage in independent and life-long learning in the broadest context of technological change.

IMSEC, GHAZIABAD

Department of Electronics and Communication Engineering

Program Educational Objectives (PEOs)

PEO1: Graduates will excel in Electronics & Communication Engineering, both in industrial and academic sector by applying their technical skills and knowledge in a professional manner.

PEO2: Graduates will be capable of effectively analyzing and solving engineering problems utilizing appropriate techniques and advanced engineering tools.

PEO3: Graduates will be capable of applying their knowledge both in individual and multidisciplinary environments. They will also demonstrate excellent communication skills and caliber to work as a team.

PEO4: Graduates will realize the significance of environmental concerns while keeping safety, ethical and societal values into consideration.

PEO5: Graduates will be capable of implementing outputs derived from research based knowledge in projects, analysis and interpretation of data leading to development of new processes and systems.

IMSEC, GHAZIABAD

Department of Electronics and Communication Engineering

PROGRAM SPECIFIC OUTCOMES (PSOs)

At the end of the program, the students will have:

1. An ability to exhibit knowledge acquired from mathematics, engineering fundamentals, Electronics & Communication engineering and related fields for professional excellence in industry and research organizations.
2. An ability to solve and communicate complex Electronics and Communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive at cost effective and appropriate solutions.
3. Wisdom of social and environmental awareness along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.
4. An ability to select appropriate techniques , resources for execution of projects and function effectively as an individual as well as a team member in multidisciplinary diverse environments.

IMS ENGINEERING COLLEGE, GHAZIABAD
ACADEMIC CALENDAR (As per AKTU) (ODD SEM: 2020 - 21) [Version-1]

Oct-20

M	T	W	T	F	S	S
			1	2	3	4
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30	31	

T/ W Days : 19/21

Nov-20

M	T	W	T	F	S	S
						1
2	3	4	5	6	7	8
9	10	11	12	13	14	15
16	17	18	19	20	21	22
23	24	25	26	27	28	29
30						

T/ W Days : (16+3)/20

Dec-20

M	T	W	T	F	S	
	1	2	3	4	5	6
7	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29	30	31			

T/ W Days : 17/24

Jan-21

M	T	W	T	F	S	S
				1	2	3
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29	30	31

T/ W Days : 15/22

Feb-21

M	T	W	T	F	S	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28

T/ W Days : 20/22

Mar-21

M	T	W	T	F	S	
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				

T/ W Days : 5/23

IMPORTANT DATES	HOLIDAYS	EXAMINATION / CLASS TEST
Commencement of Classes for 2nd, 3rd & 4th Yr: 5th Aug	14, 15 & 16 NOV (SAT, SUN & MON): Deepawali	CT-1 : 2nd-DEC to 8thDEC, 2020
Commencement of Classes for 1st & 2nd (Lateral) 25th NOV	30-NOV (MON) : Guru Nanak's B'day	CT-2 : 19, 21, 26, 28-DEC, 2, 4 JAN 2021
	25-DEC (FRI) : Christmas Day	PUT : 18th JAN to 23rd JAN, 2021
	11-MAR (THU) : Maha Shivratri	(3rd & 4th Year AKTU External)
Upload Assignment (Important Dates)	28-MAR (SUN) : Holika Dahen	AKTU End Sem Exam (01-FEB to 20-FEB, 2021)
	29-MAR (MON) : Holi	(1st & 2nd Year AKTU External)
		AKTU End Sem Exam (08-MAR to 20-MAR, 2021)
		AKTU End Sem Practical Examination

Total Teaching Days/Working Days (T/W) : 60/132 [95/132]

Faculty members are requested to 1) Upload the attendance after completion of the class (L/T/P) itself on the same day.
2) Upload / Check / Submit the assignment as per schedule (weekly).

IMS ENGINEERING COLLEGE	IMSEC/QF/08b
FORMAT	Page 1 of 1
	Issue No: 01
Time Table	Issue Date: 1 May 2010
Prepared by:	Approved by: Director

CLASS TT EC-2 4th YEAR (C-306)

Academic Session2020-21(ODD)

DAY/TIME	Period-1	Period-2	Period-3	Period-4	Break	Period-5	Period-6
	9:00-9:50	10:00-10:50	11:00-11:50	12:00-12:50	12:50-2:00 PM	2:00-2:50 PM	3:00-3:50 PM
MON			KEC 301			Electronics Devices Lab	
TUE	KEC 301	KEC 301				Integrated Circuits Lab	
WED			KEC-501				
THU		KEC 301				KEC-501	
FRI	KEC-501			KEC-501			
SAT							

CODE	Subject	FACULTY	Code	Lab Name
KEC-501	Integrated Circuits	PROF PRAVEEN KUMAR	KEC 351	Electronics Devices Lab
KEC-351	Electronic Devices	PROF PRAVEEN KUMAR	KEC-551	Integrated Circuits Lab

IMS ENGINEERING COLLEGE GHAZIABAD

ELECTRONICS & COMMUNICATION ENGINEERING DEPARTMENT

EC 3rd year

S.No.	Roll No.	Name	Student No.	Father No.
1	1714331042	RAHUL SINGH	8512846443	
2	1814331002	AASHI SINGH	9760844799	7253090799
3	1814331004	ABHISHEK KANDPAL	8929297923	9810334103
4	1814331003	ABHISHEK KUMAR	7352133304	9348555526
5	1814331005	ADITYA KUMAR	7524056794	9598271523
6	1814331006	ADITYA PANDEY	9628647442	9005808762
7	1814331007	AKHIL RUHELA	7838954908	9953004133
8	1814331008	AKSHAY VERMA	7017889514	9410267058
9	1814331009	ALI MAJAZ	8191919749	9634371978
10	1814331010	AMAN SAIFI	9897940786	9897940786
11	1814331011	ANIRUDH MANOJ	8006060404	8006060404
12	1814331012	ANMOL SHARMA	8588861488	9871589567
13	1814331013	ANSHUL SHARMA	9899062918	7428572447
14	1814331014	ANTRIKSH SAXENA	8057290569	9639971946
15	1814331015	ANUBHAV SINGH	9536712418	6396061138
16	1814331016	ARBAZ AKHTAR	7905325543	9540080461
17	1814331028	ARMAN SHAH	9910636028	9958139757
18	1814331017	ARPIT SONI	7607524723	8423002715
19	1814331018	ASHISH CHAUDHARY	7453039250	9719057509
20	1814331019	ASHISH SHARMA	9105212161	9927365600
21	1814331020	AYUSH SAINI	7060050264	9368007688
22	1814331021	HARDIK RASTOGI	8265983373	9837048602
23	1814331022	HARSH JAISWAL	7651966994	9450630124
24	1814331023	JATIN AGARWAL	8171008360	9897046135
25	1814331024	JATIN RANA	9311663355	9871023868
26	1814331025	JAYA SINHA	9354773714	8966841558
27	1814331026	KRITIKA NATH	7530845511	9971381759
28	1814331032	MANIK CHOUDHARY	8082640017	9055072582
29	1814331027	MANSI SAXENA	9794790063	9044879071
30	1814331029	MUDIT PRATAP SINGH	9415998182	9451466553

31	1814331030	MUKUL CHAUHAN	8859977600	8859977600
32	1814331031	MUNESH KUMAR SINGH	7007912346	9952709172
33	1814331033	NIKHIL KUMAR	8192828586	9410653845
34	1814331034	NISHA .	9821151993	9716598366
35	1814331035	NITESH UPADHYAY	8006041323	8006041323
36	1814331036	PRABHAT MITTAL	9457625151	9410224751
37	1814331037	PRADEEP DUBEY	9598900234	7532989975
38	1814331038	PRAKHAR TRIVEDI	9554604065	9415474508
39	1814331039	RACHIT GARG	9717182905	9667223326
40	1814331040	RISHABH GUPTA	7081168512	9026374265
41	1814331041	RIYA AGARWAL	9412659808	9837654012
42	1814331042	SAKSHI VARSHNEY	7455007178	9058464594
43	1814331043	SARANSH RAI	9682290100	9532706590
44	1814331044	SARTHAK GUPTA	9784546866	9887859633
45	1814331045	SAURABH GUPTA	8382814157	9984160785
46	1814331046	SHASHWAT DWIVEDI	9161133639	9090973080
47	1814331047	SHELENDRA RAGHAV	9868937012	8130603668
48	1814331048	SHIVAM KATIYAR	9354483513	9654958542
49	1814331049	SHIVANGI MISHRA	9532215002	8800108462
50	1814331050	SUPREET DEOL	8160586479	9927647574
51	1814331051	TANISH VARSHNEY	7906229438	9219758815
52	1814331052	TANISHKA VATS	8810335918	9599612689
53	1814331053	TUSHAR KUMAR	7906365288	7060153909
54	1814331054	UTKARSH SINGH	6351611541	7228888653
55	1814331055	VED PRAKASH SHARMA	9472207260	9631623631
56	1814331056	VISHAL RANA	7839801507	8650664356
57	1814331057	YASH DIXIT	8279724868	9917022660
58	1814331058	YASHASVI SINGH	9956441270	9918164501

B.Tech. V Semester
Electronics and Communication Engineering

S. No.	Course Code	Course Title	Periods			Evaluation Scheme				End Semester		Total	Credits
			L	T	P	CT	TA	Total	PS	TE	PE		
1	KEC-501	Integrated Circuits	3	1	0	30	20	50		100		150	4
2	KEC-502	Microprocessor & Microcontroller	3	1	0	30	20	50		100		150	4
3	KEC-503	Digital Signal Processing	3	1	0	30	20	50		100		150	4
4	KEC-051-054	Department Elective-I	3	0	0	30	20	50		100		150	3
5	KEC-055-058	Department Elective-II	3	0	0	30	20	50		100		150	3
6	KEC-551	Integrated Circuits Lab	0	0	2				25		25	50	1
7	KEC-552	Microprocessor & Microcontroller Lab	0	0	2				25		25	50	1
8	KEC-553	Digital Signal Processing Lab	0	0	2				25		25	50	1
9	KEC-554	Mini Project/Internship **	0	0	2				50			50	1
10	KNC501/KNC502	Constitution of India, Law and Engineering / Indian Tradition, Culture and Society	2	0	0	15	10	25		50			NC
11		MOOCs (Essential for Hons. Degree)											
		Total										**950**	**22**

**The Mini Project or Internship (4weeks) conducted during summer break after IV Semester and will be assessed during Vth Semester.

Course Code	Course Title
	Department Elective-I
KEC-051	Computer Architecture and Organization
KEC-052	Industrial Electronics
KEC-053	VLSI Technology
KEC-054	Advance Digital Design using Verilog
	Department Elective-II
KEC-055	Electronics Switching
KEC-056	Advance Semiconductor Device
KEC-057	Electronics Measurement & Instrumentation
KEC-058	Optical Communication

KEC-501	INTEGRATED CIRCUITS	3L:1T:0P	4 Credits

Unit	Topics	Lectures
I	**The 741 IC Op-Amp**: General operational amplifier stages (bias circuit, the input stage, the second stage, the output stage, short circuit protection circuitry), device parameters, DC and AC analysis of input stage, second stage and output stage, gain, frequency response of 741, a simplified model, slew rate, relationship between ft and slew rate.	8
II	**Linear Applications of IC Op-Amps:** Op-Amp based V-I and I-V converters, instrumentation amplifier, generalized impedance converter, simulation of inductors. **Active Analog filters:** Sallen Key second order filter, Designing of second order low pass and high pass Butterworth filter, Introduction to band pass and band stop filter, all pass active filters, KHN Filters. Introduction to design of higher order filters.	8
III	**Frequency Compensation & Nonlinearity:** Frequency Compensation, Compensation of two stage Op-Amps, Slewing in two stage Op-Amp. Nonlinearity of Differential Circuits, Effect of Negative feedback on Nonlinearity. **Non-Linear Applications of IC Op-Amps:** Basic Log–Anti Log amplifiers using diode and BJT, temperature compensated Log-Anti Log amplifiers using diode, peak detectors, sample and hold circuits. Op-amp as a comparator and zero crossing detector, astable multivibrator & monostable multivibrator. Generation of triangular waveforms, analog multipliers and their applications.	4 8
IV	**Digital Integrated Circuit Design:** An overview, CMOS logic gate circuits basic structure, CMOS realization of inverters, AND, OR, NAND and NOR gates. **Latches and Flip flops**: the latch, CMOS implementation of SR flip-flops, a simpler CMOS implementation of the clocked SR flip-flop, CMOS implementation of J-K flip-flops, D flip- flop circuits.	6
V	**Integrated Circuit Timer:** Timer IC 555 pin and functional block diagram, Monostable and Astable multivibrator using the 555 IC. Voltage Controlled Oscillator: VCO IC 566 pin and functional block diagram and applications. **Phase Locked Loop (PLL)**: Basic principle of PLL, block diagram, working, Ex-OR gates and multipliers as phase detectors, applications of PLL.	6

Text Book:

1. Microelectronic Circuits, Sedra and Smith, 7th Edition, Oxford, 2017.
2. Behzad Razavi: Design of Analog CMOS Integrated Circuits, TMH

Reference Books:

1. Gayakwad: Op-Amps and Linear Integrated Circuits, 4th Edition Prentice Hall of India, 2002.
2. Franco, Analog Circuit Design: Discrete & Integrated, TMH, 1st Edition.
3. Salivahnan, Electronics Devices and Circuits, TMH, 3rd Edition, 2015
4. Millman and Halkias: Integrated Electronics, TMH, 2nd Edition, 2010

Course Outcomes: At the end of this course students will demonstrate the ability to:

1. Explain complete internal analysis of Op-Amp 741-IC.
2. Examine and design Op-Amp based circuits and basic components of ICs such as various types of filter.
3. Implement the concept of Op-Amp to design Op-Amp based non-linear applications and wave-shaping circuits.
4. Analyse and design basic digital IC circuits using CMOS technology.
5. Describe the functioning of application specific ICs such as 555 timer ,VCO IC 566 and PLL.

Lecture No 17

18 September 2020

Error correction possible

Hamming Code Hamming code is an error-correcting code. It is constructed by adding a number of parity bits to each group of n-bit information, or message in such a way so as to be able to locate the bit position in which error occurs. Let us assume that k parity bits $p_1, p_2 \ldots, p_k$ are added to the n-bit message to form an $(n + k)$-bit code. The value of k must be chosen in such a way so as to be able to describe the location of any of the $n + k$ possible error bit locations and also 'no error' condition. Consequently, k must satisfy the inequality

$$2^k \geq n + k + 1. \tag{2.2}$$

The location of each of the $n + k$ bits within a code word is assigned a decimal number, starting from 1 to the *MSB* and $n + k$ to the *LSB*. k parity checks are performed on selected bits of each code word. Each parity check includes one of the parity bits. The result of each parity check is recorded as 1 if error has been detected and as 0 if no error has been detected. Let the results of the parity checks involving the parity bits $p_k, p_{k-1}, \ldots$ are $c_1, c_2, \ldots$ respectively. Bit c_1 is 1 if an error is detected and 0 if there is no error. Similarly $c_2, c_3, \ldots$, etc. The decimal value of the binary word formed $c_1, c_2 \ldots, c_k$ gives the decimal value assigned to the location of the erroneous bit. If there is no error, then the decimal value will be 0. This decimal number is the position or location number. The parity bits $p_1, p_2, \ldots$ are placed in locations $1, 2, 4, \ldots, 2^{k-1}$.

data is n bits
add K bits
Parity
total bits n+k

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Example 2.45

Find out the value of k for converting BCD code into Hamming code and the bit positions of the resulting Hamming code.

Solution

The value of k must be chosen to satisfy the eqn. (2.2) since $n = 4$, therefore,

$$2^k \geq k + 5$$

$2^K \geq n + K + 1$

$2^K \geq 4 + K + 1$

$K = 3$

The minimum value of k for which it is satisfied is 3. Therefore, three parity bits are attached to each of the BCD code for constructing the Hamming code. It will be a 7-bit code with bit positions

p_1	p_2	n_1	p_3	n_2	n_3	n_4
1	2	3	4	5	6	7

2^0

Parity

$d_3 d_2 d_1 P_3 d_0 P_2 P_1$

data bits

Values (0 or 1) are assigned to the parity bits so as to make the Hamming code have either even parity or odd parity and when an error occurs, the position number will take on the value assigned to the location of the erroneous bit.

In the case of BCD code with three parity bits there are seven error positions. Table 2.13 gives these error

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p_3 is selected so as to establish even (or odd) parity in positions 4, 5, 6, 7

$h_1 h_2 h_3 h_4$

0110

Example 2.46

Construct Hamming code for BCD 0110. Use even parity.

$p_1 = h_1 \oplus h_2 \oplus h_4$

Solution

For 4-bit code three parity bits p_1, p_2, and p_3 are appended in locations 1, 2, and 4 respectively as shown below:

Position	1	2	3	4	5	6	7
	p_1	p_2	n_1	p_3	n_2	n_3	n_4
Original BCD			0		1	1	0
Even parity in positions 1, 3, 5, 7 requires $p_1 = 1$	1		0		1	1	0
Even parity in positions 2, 3, 6, 7 requires $p_2 = 1$	1	1	0		1	1	0
Even parity in positions 4, 5, 6, 7 requires $p_3 = 0$	1	1	0	0	1	1	0

$p_2 = h_1 \oplus h_3 \oplus h_4$

Total no 1's → one

$p_3 = h_2 \oplus h_3 \oplus h_4$

Therefore, Hamming code for BCD digit 0110 with even parity is 1100110.

2020-09-18 10:26:43

IMS Engineering College Ghaziabad

Department of Electronics & Communication Engineering

* Required

1. Email address *

Quiz

Subject Name :-Digital System Design

Subject Code :- KEC 302

2. Roll No. *

3. Name *

Important Instructions

1. All questions are compulsory. Each question carry one mark.
2. You are allowed to submit only once, therefore verify your answers before submission.
3. Do not submit using multiple email ids, this may lead to cancellation of your exam.

4. A D flip flop can be constructed from which flip flop by using an additional NOT gate. * 1 point

Mark only one oval.

- S-R
- Both J-K and S-R
- J-K
- T

5. Determine the characteristic equation of T flip flop? * 1 point

Mark only one oval.

- Qn+1=Tn.Qn' + Tn'.Qn
- Qn+1=Tn.Qn + Tn'.Qn
- Qn+1=Tn.Qn + Tn'.Qn'
- Qn+1=Tn + Tn'.Qn

6. Which of the following flip flop is not free from race around condition? * 1 point

Mark only one oval.

- D Flip Flop
- T Flip Flop
- JK Flip Flop
- Master Slave JK Flip Flop

7. Question * 1 point

Consider the following state table:

Present state	Next state		Output	
	X = 0	X = 1	X = 0	X=1
a	a	b	0	1
b	c	d	0	0
c	a	d	0	1
d	e	f	1	0
e	a	f	1	0
f	g	f	1	0
g	a	f	1	0

Which of the following statements are TRUE?

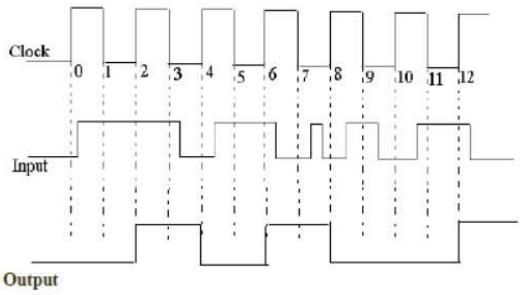
I. The state table corresponds to a Mealy Machine.
II. The number of states can be reduced to a minimum of 5 states.
III. The number of states can be reduced to a minimum of 6 states.
IV. States 'd', 'e', 'f' and 'g' are equivalent.
V. States 'd' and 'f' are equivalent.

Mark only one oval.

- III, IV, V only
- I, III, IV only
- I, II, V only
- II, IV, V only

8. Question * 1 point

The waveform indicates the operation of

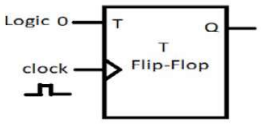


Mark only one oval.

- Negative edge triggered J-K Flip Flop
- Positive edge triggered S-R Flip Flop
- Positive edge triggered D Flip Flop
- Negative edge triggered T Flip Flop

9. * 1 point

What is the output frequency of the following circuit for 5MHz clock signal?
(Assume initial values of Q is logic 1)

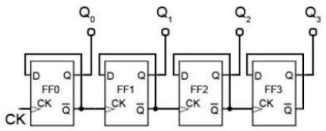


Mark only one oval.

- 5 MHz
- 0 MHz
- 10 MHz
- 2.5 MHz

10. Question * 1 point

Identify the outputs of the following circuit after five clock transitions. The initial values of all flip-flops are 0.

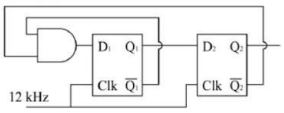


Mark only one oval.

- Q3 Q2 Q1 Q0 = 0101
- Q3 Q2 Q1 Q0 = 0000
- Q3 Q2 Q1 Q0 = 0011
- Q3 Q2 Q1 Q0 = 1100

11. Question * 1 point

In the circuit shown, the clock frequency, i.e., the frequency of the Clk signal, is 12 kHz. The frequency of the signal at Q2 is _____ kHz.

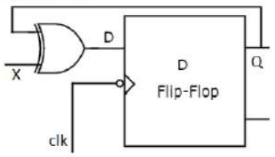


Mark only one oval.

- 12 kHz
- 3 kHz
- 4 kHz
- 36 kHz

12. Question * 1 point

Identify the operation of following circuit.



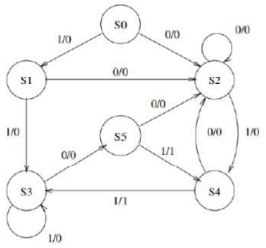
Mark only one oval.

- D Flip Flop
- T Flip Flop
- SR Flip Flop
- JK Flip Flop

13. Question * 1 point

Let X is the input sequence whereas Z is the output sequence for the state machine shown below. Which of the following options correctly describes the output Z sequence for input sequence X given below (Assume initial state S0)

X = 1 0 1 1 0 0 1



Mark only one oval.

- Z = 1011001
- Z = 0100110
- Z = 0001000
- Z= 0000100

14. CMOS is not preferred for * 1 point

Mark only one oval.

- Low power dissipation
- Small size
- Good immunity to noise
- High switching speed

15. Which of the following has the highest noise margin * 1 point

Mark only one oval.

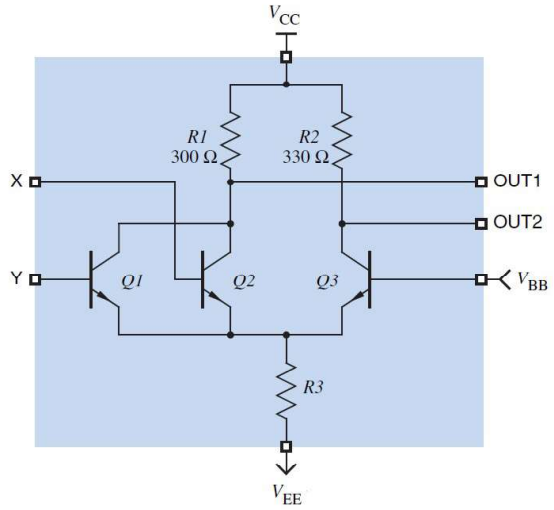
- TTL
- RTL
- ECL

16. Which of the following has highest speed * 1 point

Mark only one oval.

- TTL
- CML
- CMOS
- RTL

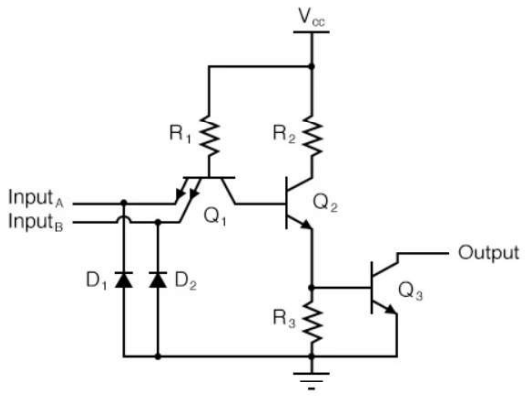
17. The following is a circuit of * 1 point



Mark only one oval.

- RTL NOR/OR gate
- TTL NOR/OR gate
- ECL NOR/OR gate
- CMOS NOR/OR gate

18. The following is a circuit of * 1 point



Mark only one oval.

- RTL NOR gate
- TTL NAND Gate
- ECL NOR/OR gate
- RTL NAND gate
- TTL NOR gate

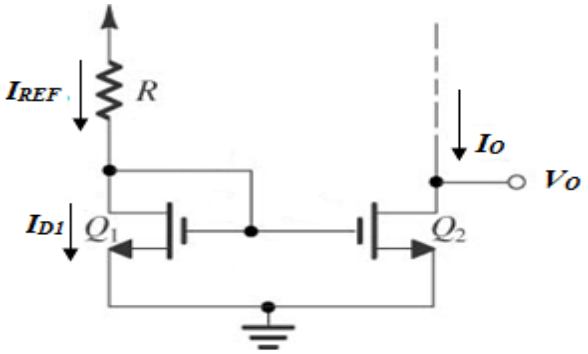
Subject Name : Integrated Circuits	Subject Code	REC-501
Date of Handout : 09-08-2019	Max Marks	
Date of Submission :14-08-2019		

ASSIGNMENT 1

Q.1. Explain MOSFET current mirror, also show the effect of V_o on I_o.

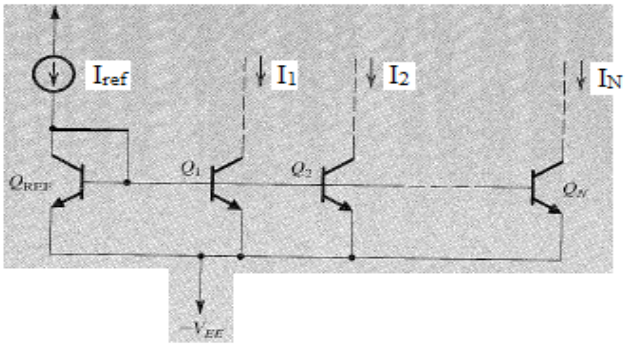
Q.2. Describe BJT current mirror and show the effect of finite β on the Current transfer ratio.

Q.3. For V_{dd} = 1.8V and using I_{REF} = 50µA. It is required to design the circuit of following fig. to obtain an output current whose nominal value is 50µA. Find R if Q_1 and Q_2 are matched with channel lengths of 0.5µm, channel widths of 5µm, V_t = 0.5V and k_n' = 250µA/V^2.What is the lowest possible value of V_o? Assuming that for this process technology the early voltage V'$_A$ = 20V/µm, find the output resistance of current source.



Q.4. Following Fig. shows an N output current mirror. Assuming that all transistors are matched and have finite β and ignoring the effect of finite output resistances, show that

$$I_1 = I_2 = \ldots I_N = \frac{Iref}{1+\frac{N+1}{\beta}}$$



For β = 100, find the maximum number of outputs for an error not exceeding 10%.

Subject Name : IC	Subject Code	REC-501
Date of Handout : 16.08.2019	Max Marks	
Date of Submission : 23.08.2019		

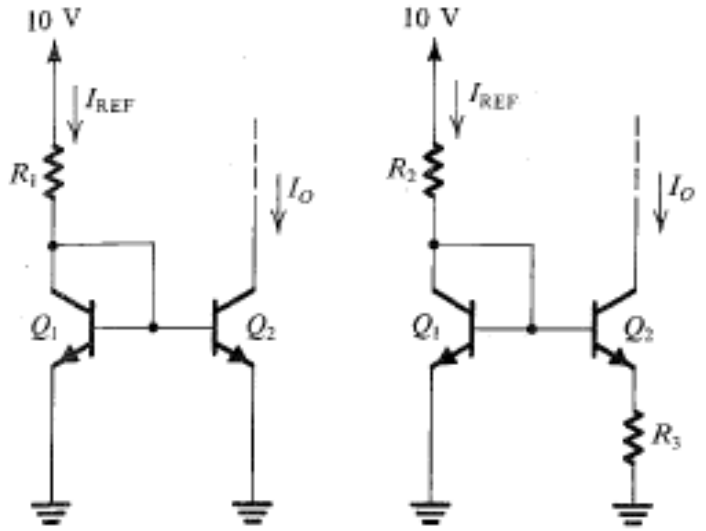
ASSIGNMENT 2

Q.1. Explain Wilson MOS mirror. Also draw the circuit of improved Wilson mirror.

Q.2. Draw the circuit of a bipolar mirror with base current compensation. Explain how it reduces the effect of β on current transfer ratio of current mirror.

Q.3. Explain the cascode current mirror. Write the advantage and disadvantage of the cascode current mirror.

Q.4. Explain Widlar current source.
Following figure (a) and (b) shows the two circuit for generating a constant current of 10μA which operates from 10V supply. Determine the value of required resistors assuming that V_{BE} = 0.7V at a current of 1mA and neglecting the effect of finite β.



(a) (b)

Subject Name : Integrated Circuits	Subject Code	REC-501
Date of Handout : 30-09-2019	Max Marks	
Date of Submission : 09-09-2019		

ASSIGNMENT 3

Q.1 Draw the circuit diagram of CMOS inverter and explain its transfer characteristics.

Q.2 List the advantage of CMOS logic family

Q.3 Draw the CMOS realization of the following Boolean expression

a) $Y = \overline{A + B(C + D}$ b) $Y = \overline{(A + B).C + D}$

c) $Y = \overline{A + (B + C) + D.E}$ d) $Y = AB + \bar{A}\bar{B}$ e) $Y = AB + C$

Q.4 Discuss the features of CMOS circuit. Realize one AND-OR-INVERT (AOI) and one OR- AND-INVERT (OAI) function using CMOS logic circuit.

Q.5 Design a CMOS full adder circuit with three inputs A, B, C and two output S and C_o.

Q.6 Give a CMOS logic circuit that realizes the function of three input odd parity checker. Specificially, the output is to be high when an odd number (1 or 3) of the input are high. Attempt a design with 10 transistors (not counting those in the inverters) in each of the PUN and PDN.

Subject Name : Integrated Circuit	Subject Code	REC-501
Date of Handout : 13-09-2019	Max Marks	
Date of Submission : 19-09-2019		

ASSIGNMENT 4

Q.1 For a process technology with L=0.5µm, n=1.5, p=6. Give size of all transistors in (i) a four input NOR and (ii) a four input NAND Gate. Also compare the area of two Gates and then shows that CMOS NAND is preferred over CMOS NOR.

Q.2 Determine the W/L ratios for all transistor used in CMOS implementation of the function $Y = \overline{A(B + CD)}$

Q.3 Give the CMOS implementation of clocked SR flip-flop and explain its working.

Q.4 Draw the D-flip flop using CMOS. Also draw and explain its master slave configuration.

Subject Name	: Integrated Circuit	Subject Code	REC-501
Date of Handout	: 27-09-2019	Max Marks	
Date of Submission	: 03-10-2019		

ASSIGNMENT 5

Q.1 Define the following term with reference to op-amp
(i) CMRR (ii) Slew rate (iii) PSRR
(iv) Input offset voltage (v) Bias current

Q.2 Realize generalized impedance converter (GIC) with op-amp. How the inductor is simulated using this GIC.

Q.3 Draw a second order low-pass and high pass filter and drive its transfer function. Design a second order low pass butterworth filter having upper cut-off frequency of 1kHz and a passband gain of 2

Q.4 Derive the expression of voltage gain in KHN biquad filter.

Q.5 Draw the following Circuit using op-amp
(i) Weighted Summer (ii) Difference Amplifier
(iii) V-I converter (iv) I-V Converter

Subject Name : Integrated Circuit	Subject Code	REC-501
Date of Handout : 18-10-2019	Max Marks	
Date of Submission : 23-10-2019		

ASSIGNMENT 6

Q.1 Draw and explain the circuit of temperature compensated logarithmic amplifier.

Q.2 Draw and explain the circuit of temperature compensated anti-logarithmic amplifier.

Q.3 Draw and explain the circuit diagram of precision full wave rectifier.

Q.4 Explain inverting and non-inverting Schmitt trigger.

Q.4 Draw and explain the circuit of square wave generator circuit using op-amp.

Subject Name : Integrated Circuit	Subject Code	REC-501
Date of Handout : 08-11-2019	Max Marks	
Date of Submission : 15-11-2019		

ASSIGNMENT 7

Q.1 Draw the functional block diagram of IC 555 and explain its working.

Q.2 Draw and explain monostable multivibrator using 555 timer and calculate its pulse width period.

Q.3 Draw and explain astable multivibrator using 555 timer and find the free running frequency of the output.

Q.4 An 8bit DAC has an input of 10011011 and 10V reference, find the corresponding output voltage.

Q.5 The basic step of a 8-bit DAC is 20mV. If 00000000 represents 0V, what is represented by the input 10110111.

Q.6 Explain the operation of Dual slope ADC.

(http://52.66.16.110/user)

Dashboard (http://52.66.16.110/user#/dashboard)

Module (http://52.66.16.110/user#/module_list)

Assignment

Assignment

Student Wise Assignment Report

Faculty Wise Assignment Report

Section Wise Assignment Report

Assignment Report

Course: B.Tech

Stream: Electronics & Communication

Year: 3 Year

Subject: Integrated Circuits (KEC 501)

Section: EC1

#	Registered	Batch	Status	Roll No	Student Name	Assignment 07	Assignment 06	Assignment 05	Assignment 04	Assignment 03	Assignment 02	Assignment 01	Total
1	Yes	EC1	Regular	1714331042	RAHUL SINGH	1	0	1	1	1	1	1	6
2	Yes	EC1	Regular	1814331002	AASHI SINGH	1	1	0	1	1	1	1	6
3	Yes	EC1	Regular	1814331003	ABHISHEK KUMAR	1	1	1	1	1	1	1	7
4	Yes	EC1	Regular	1814331004	ABHISHEK KANDPAL	1	1	1	1	1	1	1	7
5	Yes	EC1	Regular	1814331005	ADITYA KUMAR	1	1	1	1	1	1	0	6
6	Yes	EC1	Regular	1814331006	ADITYA PANDEY	1	1	1	1	1	1	1	7
7	Yes	EC1	Regular	1814331007	AKHIL RUHELA	1	1	1	1	1	1	1	7
8	Yes	EC1	Regular	1814331008	AKSHAY VERMA	1	1	1	0	1	1	1	6
9	Yes	EC1	Regular	1814331009	ALI MAJAZ	1	1	1	1	1	1	1	7
10	Yes	EC1	Regular	1814331010	AMAN SAIFI	1	1	1	1	1	1	1	7
11	Yes	EC1	Regular	1814331011	ANIRUDH MANOJ	0	0	0	1	1	1	1	4
12	Yes	EC1	Regular	1814331012	ANMOL SHARMA	1	1	1	1	1	1	1	7
13	Yes	EC1	Regular	1814331013	ANSHUL SHARMA	1	1	1	1	1	1	1	7
14	Yes	EC1	Regular	1814331014	ANTRIKSH SAXENA	1	1	1	1	1	1	1	7
15	Yes	EC1	Regular	1814331015	ANUBHAV SINGH	1	1	1	1	1	1	1	7
16	Yes	EC1	Regular	1814331016	ARBAZ AKHTAR	1	1	1	1	1	1	1	7
17	Yes	EC1	Regular	1814331017	ARPIT SONI	1	1	1	1	1	1	1	7
18	Yes	EC1	Regular	1814331018	ASHISH CHAUDHARY	1	1	0	1	1	1	1	6
19	Yes	EC1	Regular	1814331019	ASHISH SHARMA	1	1	1	1	1	1	1	7
20	Yes	EC1	Regular	1814331020	AYUSH SAINI	0	1	0	0	1	1	1	4
21	Yes	EC1	Regular	1814331021	HARDIK RASTOGI	1	1	1	1	1	1	1	7
22	Yes	EC1	Regular	1814331022	HARSH JAISWAL	1	1	1	1	1	1	1	7
23	Yes	EC1	Regular	1814331023	JATIN AGARWAL	1	1	1	1	1	1	1	7
24	Yes	EC1	Regular	1814331024	JATIN RANA	1	1	1	1	1	1	1	7

(http://52.66.16.110/user)

Dashboard (http://52.66.16.110/user#/dashboard)

Module (http://52.66.16.110/user#/module_list)

Assignment

Assignment

Student Wise Assignment Report

Faculty Wise Assignment Report

Section Wise Assignment Report

#	Registered	Batch	Status	Roll No	Student Name	Assignment 07	Assignment 06	Assignment 05	Assignment 04	Assignment 03	Assignment 02	Assignment 01	Total
25	Yes	EC1	Regular	1814331025	JAYA SINHA	1	1	1	1	1	1	1	7
26	Yes	EC1	Regular	1814331026	KRITIKA NATH	1	1	1	1	1	1	0	6
27	Yes	EC1	Regular	1814331027	MANSI SAXENA	1	1	1	1	1	1	1	7
28	Yes	EC1	Regular	1814331028	ARMAN SHAH	1	1	1	1	1	1	1	7
29	Yes	EC1	Regular	1814331029	MUDIT PRATAP SINGH	1	1	1	1	1	1	1	7
30	Yes	EC1	Regular	1814331030	MUKUL CHAUHAN	1	1	1	1	1	1	1	7
31	Yes	EC1	Regular	1814331031	MUNESH KUMAR SINGH	1	1	0	1	0	1	1	5
32	Yes	EC1	Regular	1814331032	MANIK CHOUDHARY	1	1	1	1	1	1	1	7
33	Yes	EC1	Regular	1814331033	NIKHIL KUMAR	0	1	1	1	1	1	1	6
34	Yes	EC1	Regular	1814331034	NISHA .	1	1	1	1	1	1	1	7
35	Yes	EC1	Regular	1814331035	NITESH UPADHYAY	1	1	1	1	1	1	1	7
36	Yes	EC1	Regular	1814331036	PRABHAT MITTAL	1	1	1	1	1	1	1	7
37	Yes	EC1	Regular	1814331037	PRADEEP DUBEY	1	1	1	1	1	1	1	7
38	Yes	EC1	Regular	1814331038	PRAKHAR TRIVEDI	1	0	0	0	1	1	0	3
39	Yes	EC1	Regular	1814331039	RACHIT GARG	1	1	1	1	1	1	1	7
40	Yes	EC1	Regular	1814331040	RISHABH GUPTA	1	0	1	1	1	1	1	6
41	Yes	EC1	Regular	1814331041	RIYA AGARWAL	1	1	1	1	1	1	1	7
42	Yes	EC1	Regular	1814331042	SAKSHI VARSHNEY	1	1	1	1	1	1	1	7
43	Yes	EC1	Regular	1814331043	SARANSH RAI	1	1	1	1	1	1	1	7
44	Yes	EC1	Regular	1814331044	SARTHAK GUPTA	1	1	1	1	1	1	1	7
45	Yes	EC1	Regular	1814331045	SAURABH GUPTA	1	1	1	1	1	1	1	7
46	Yes	EC1	Regular	1814331046	SHASHWAT DWIVEDI	0	1	1	1	1	1	1	6
47	Yes	EC1	Regular	1814331047	SHELENDRA RAGHAV	1	0	0	0	1	1	0	3
48	Yes	EC1	Regular	1814331048	SHIVAM KATIYAR	1	1	1	1	1	1	1	7
49	Yes	EC1	Regular	1814331049	SHIVANGI MISHRA	1	1	1	1	1	1	1	7
50	Yes	EC1	Regular	1814331050	SUPREET DEOL	1	1	1	1	1	1	1	7
51	Yes	EC1	Regular	1814331051	TANISH VARSHNEY	1	1	1	1	1	1	1	7
52	Yes	EC1	Regular	1814331052	TANISHKA VATS	1	1	1	1	1	1	1	7
53	Yes	EC1	Regular	1814331053	TUSHAR KUMAR	1	1	1	1	1	1	1	7
54	Yes	EC1	Regular	1814331054	UTKARSH SINGH	0	1	1	1	1	1	1	6
55	Yes	EC1	Regular	1814331055	VED PRAKASH SHARMA	1	1	1	1	1	1	1	7
56	Yes	EC1	Regular	1814331056	VISHAL RANA	1	1	1	1	1	1	1	7

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- Dashboard (http://52.66.16.110/user#/dashboard)
- Module (http://52.66.16.110/user#/module_list)
- **Assignment**
  - Assignment
  - Student Wise Assignment Report
  - Faculty Wise Assignment Report
  - Section Wise Assignment Report

#	Registered	Batch	Status	Roll No	Student Name	Assignment 07	Assignment 06	Assignment 05	Assignment 04	Assignment 03	Assignment 02	Assignment 01	Total
57	Yes	EC1	Regular	1814331057	YASH DIXIT	1	1	0	0	0	0	0	2
58	Yes	EC1	Regular	1814331058	YASHASVI SINGH	1	1	1	1	1	1	1	7

IMS ENGINEERING COLLEGE, GHAZIABAD

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MONTHLY REPORT

Syllabus covered and assignment report

Date: 19-03-15

Year/ semester: EC2 4th Yr

Section: EC1/EC2/2EC

Name of coordinator: Praveen kumar

Subject code	Subject name	Faculty name	Unit covered(%) /total unit	no of assignment	No. of lectures proposed/ held	signature
EEC 801	Mobile & Wireless Comm.	Abhishek Sharma	2.0	3 (Three)	26	Abhishek
EEC035	Intro. to Radar Systems	Praveen Kr	2.0	3	31	kumar
EOE081	NCER	Mukesh Khandelwal	2.0	2	33	
EEC802	Electronics switching	J.N. Vashishth	2.6	4	30	Jay

kumar

(Praveen kumar)

Signature

Year coordinator

IMS ENGINEERING COLLEGE, GHAZIABAD

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MONTHLY REPORT

Syllabus covered and assignment report

Date:

Year/ semester: 2nd year/ 4th semester

Section: EC1/EC2/2EC

Name of coordinator: Akanksha Shukla

Subject code	Subject name	Faculty name	Unit covered(%)/total unit	no of assignment	No. of lectures proposed/ held	signature
NEC-402	Electronic circuits	Praveen kumar	47%	4	38	
NEC-408	Electronic measurement and instrumentation	Akashdeep	45%	4	22	
NEC-404	EMFT	Manish Zadoo	40%	4	35	
NAS-401	Engg. Mathematics-III	Solabh	40%	4	36	
NEC-401	Data structure	Kirti	40%	2	30	Kirti
NHU-402	Industrial Psychology	Akanksha Shukla	50%	4	19	
AUC-001	Human Values & Professional Ethics	Ankita Bhardwaj	40%	4	06	

Ashukla EC-1

(Akanksha Shukla)

Signature

Year coordinator

IMS ENGINEERING COLLEGE, GZB		
Sessional Question Paper	IMSEC/QF/49	
	Page 1 of 1	
	Issue no: 02	
	Issue date: 1 May 2010	
1st Sessional Examination (CT-1), Odd Sem. 2019-20		
Subject Name: Integrated Circuits	Subject code	REC 501
Roll No. of student	Max Marks	30
	Max time	1:30hrs
For EC1, EC2 3rd Year	Approved By Director	

Note: Attempt any ***six*** questions (6×5=30)

Q.1 What are the desirable characteristics of current mirror circuit? Draw the simple BJT current mirror circuit and derive the expression of current transfer ratio.

Q.2 For V_{dd} = 1.8V and using I_{REF} = 50μA. It is required to design the circuit of Fig.1 to obtain an output current whose nominal value is 50μA. Find R if Q_1 and Q_2 are matched with channel lengths of 0.5μm, channel widths of 5μm, V_t = 0.5V and k_n' = 250μA/V². What is the lowest possible value of V_o? Assuming that for this process technology the early voltage V'_A = 20V/μm, find the output resistance of current source.

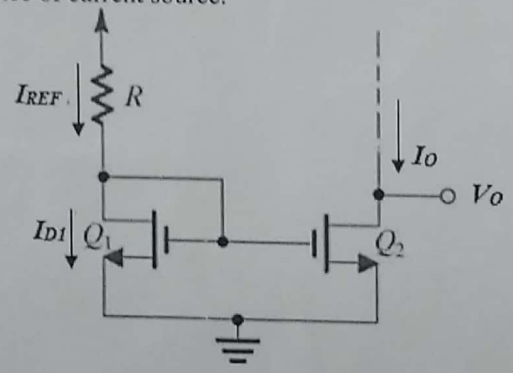


Fig.1

Q.3 Explain Wilson Current mirror. How the V_{DS} mismatching is avoided by improved Wilson mirror?

Q.4 Draw the circuit diagram of cascode current mirror; also write the advantage and disadvantage of cascode current mirror.

Q.5 Design a CMOS full adder circuit with inputs A, B, C and two output S and C_0.

Q.6 Sketch the CMOS realization of the following Boolean function-

(a) $Y = \overline{(A+B+C).D}$ (b) $Y = \bar{A}B + A\bar{B}$

Q.7 Sketch the CMOS implementation of SR flip-flop and explain its working.

Q.8 Draw the D-flip flop using CMOS. Also draw and explain its master slave configuration.

For office use only					
Course Outcomes and Question mapping matrix					
CO1	CO2	CO3	CO4	CO5	CO6
Q. 1, 2, 3, 4	-	Q. 5, 6, 7, 8	-	-	-

Shanker 30/08/19

IMSENGINEERINGCOLLEGE,GZB		
Sessional Question Paper	IMSEC/QF/49	
	Page 1 of 1	
	Issue no: 02	
	Issue date:1 May 2010	
2nd Sessional Examination (CT-2), Odd Sem. 2019-20		
Subject Name: Integrated Circuits	Subject code	REC 501
Roll No. of student	Max Marks	30
	Max time	1:30hrs
For EC1, EC2 3rd Year	Approved By Director	

Note: Attempt any ***six*** questions (6×5=30)

Q.1 Draw the generalized impedance converter and derive its impedance equation. Also simulate an Inductor.

Q.2 Explain how a Schmitt Trigger circuit works with a neat diagram. Design a Schmitt trigger with V_{UT} = 2V, V_{LT} = -2V. Assume ± V_{sat} = ±13V.

Q.3 Draw the circuit of Sallen Key filter and derive the expression of its transfer function. Also design the equal component Sallen key high pass filter.

Q.4 Derive the expression of voltage gain in KHN biquad filter. Draw the KHN biquad filter and drive transfer function of the BPF and LPF from that.

Q.5 Draw and explain basic logarithmic amplifier. Also explain temperature compensated logarithmic amplifier.

Q.6 Explain the working of precision full wave rectifier with necessary waveform.

Q.7 Design a wide band pass filter with f_l = 500Hz, f_h = 1500Hz and a pass band gain of 4. Draw frequency response of band pass filter and find value of Q.

Q.8 Design a 2nd order low pass Butterworth filter with cut off frequency of 1 KHz.

For office use only					
Course Outcomes and Question mapping matrix					
CO1	CO2	CO3	CO4	CO5	CO6
-	Q. 3, 4, 7, 8	-	Q.2, 5, 6	-	Q.1

07/11/19

IMSENGINEERINGCOLLEGE,GZB		
Sessional Question Paper	IMSEC/QF/49	
	Page 1 of 1	
	Issue no: 02	
	Issue date:1 May 2010	
PUT Examination, Odd Sem. 2019-20		
Subject Name: Integrated Circuits	Subject code	REC 501
Roll No. of student	Max Marks	70
	Max time	3 Hrs
Prepared By: MR	Approved By Director	

Note: All sections are compulsory. If require any missing data; then choose suitably.

Section-A

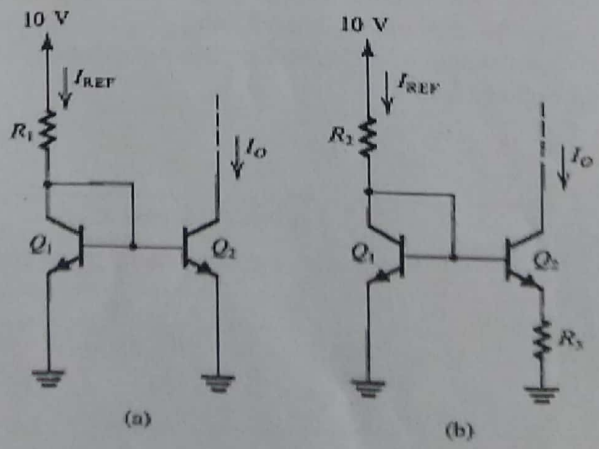
Q.1 Attempt any **seven** parts of this question (2×7=14)

a) What is the advantage of Widlar current source over simple constant current source?
b) Define and give significance of Slew Rate.
c) Write the advantage of active filter over passive filter?
d) What do you mean by a frequency response of a filter circuit?
e) Why CMOS NAND is preferred over CMOS NOR?
f) Give two application of analog multiplier.
g) What is a Super Diode?
h) List the application of PLL.
i) The basic step of a 8-bit DAC is 20mV. If 00000000 represents 0V, what is represented by the input 10110111.
j) What are the advantages of CMOS logic family?

Section-B

Attempt any ***three*** questions of this section. (7×3=21)

Q.2 Explain Widlar current source.
Following Fig. (a) and (b) shows the two circuit for generating a constant current of 10μA which operates from 10V supply. Determine the value of required resistors assuming that $V_{BE} = 0.7V$ at a current of 1mA and neglecting the effect of finite β.



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Q.3 Draw the CMOS realization of the following Boolean expression
(i) $Y = \overline{A + B(C + D)}$ (ii) $Y = \overline{(A + B).C + D}$

Q.4 Explain the circuit of following current mirror and also discuss their advantage-
(i) Wilson current mirror (ii) Base current compensated current mirror

Q.5 Explain the following circuit using op-amp
(i) Schmitt trigger (ii) Comparator and zero crossing detector

Q.6 (i) Design a wide band pass filter with f_L = 200Hz, f_H =1KHz and a pass band gain of 4.
(ii) Design a 2nd order Butterworth high pass filter with cut-off frequency of 1KHz.

Q.7 Explain R-2R ladder type digital to analog converter.

Section-C

Attempt ***any one part*** of each questions of this section. (7×5=35)

Q.8 a) Discuss the frequency response of 741opamp. Relate unity-gain bandwidth and slew rate.
b) How the short circuit protection is achieved in the output stage of 741 op-amp?
c) Explain MOSFET current mirror, also show the effect of V_o on I_o.

Q.9 a) Draw the circuit of KHN biquad filter and derive the expression of its voltage gain
b) Realize generalized impedance converter (GIC) with op-amp. How the inductor is simulated using this GIC.
c) Implementation the following filter using op-amp
(i) Notch filter (ii) Narrow band pass filter

Q.10 a) Design a CMOS full adder circuit with three inputs A, B, C and two output S and C_o.
b) Give the CMOS implementation of clocked SR flip-flop and explain its working.
c) Draw the D-flip flop using CMOS. Also draw and explain its master slave configuration.

Q.11 a) Draw and explain the circuit of temperature compensated logarithmic amplifier.
b) Explain working of precision full wave rectifier with necessary waveform.
c) Draw and explain the circuit of square wave generator (astable multivibrator) using op-amp and derive the expression of output frequency.

Q.12 a) Explain the operation of dual slope ADC.
b) Draw and explain the circuit of astable multivibrator using 555 timer. Also derive the expression of frequency and duty cycle of output wave form.
c) Draw the block diagram of a PLL and explain its operation. Explain lock-in-range, capture range and pull-in time of a PLL.

For office use only					
Course Outcomes and Question mapping matrix					
CO1	CO2	CO3	CO4	CO5	CO6
Q.1(a,b), Q.2, Q.4, Q.8	Q.1(c,d), Q.6, Q.9	Q.1(e,j), Q.3, Q.10	Q.1(f, g), Q.5, Q.11	Q.1(i), Q.7, Q.12 (a,c)	Q.1(h), Q.12(b)

IMS Engineering College, Ghaziabad
Department of Electronics & Communication Engineering
PUT Result Analysis (Odd Semester 2019-20)

Class: EC1 3rd Year — Sub: Integrated Circuits (REC 501)

S. No.	University Roll	Name	CT-1 Marks (30)	CT-1 Marks (30)	PUT Marks (70)
1	1714331001	ABHISHEK PATEL	12	13	47
2	1714331002	ADARSH KUMAR JHA	12	20	55
3	1714331003	AKSHANSH SINGH	14	AB	35
4	1714331004	AMAN KANSAL	12	3	36
5	1714331005	AMAN SINGH ASWAL	13	AB	41
6	1714331006	AMAN DESHWAL	12	AB	23
7	1714331007	AMIT YADAV	12	3	39
8	1714331008	ANJU SINGH	12	AB	30
9	1714331009	ANMOL LATIYAN	7	AB	7
10	1714331010	ANOOP KUMAR MISHRA	8	AB	50
11	1714331011	ANUJ SINGH	8	10	33
12	1714331012	ANUSHK SRIVASTAV	19	AB	37
13	1714331013	ARIHANT JAIN	AB	AB	32
14	1714331014	ASHISH KUMAR DUBEY	15	24	55
15	1714331015	ATUL KUMAR	AB	AB	5
16	1714331016	AYUSH AWASTHI	12	16	35
17	1714331017	CHAKSHU PARASHAR	10	AB	18
18	1714331018	GAURAV THAPLIYAL	0	3	10
19	1714331019	HARSHIT TOMAR	13	AB	28
20	1714331020	HIMANSHU GANGWAR	5	AB	10
21	1714331021	JANMEJAY SINGH CHAUHAN	21	AB	35
22	1714331022	JAYDEEP AGARWAL	23	AB	67
23	1714331023	KARAN SHARMA	13	23	47
24	1714331024	KARTIK SINGHAL	2	2	22
25	1714331025	KM. SHIVANGI AGRAWAL	26	AB	56
26	1714331026	KRISHNA MURARI RAI	5	7	34
27	1714331027	KULDEEP SINGH	12	AB	37
28	1714331029	MEGHA VISHWAKARMA	21	AB	28
29	1714331030	MUDIT GARG	8	AB	40
30	1714331031	MUKUL SINGH SISODIA	4	10	25
31	1714331032	NEERAJ KUMAR	12	AB	33
32	1714331034	NISHI GUPTA	28	AB	48
33	1714331035	NITIN KUMAR YADAV	4	4	16
34	1714331038	PIYUSH KUMAR SINGH	18	AB	39
35	1714331075	YATI SHINGAL	28	23	65

Number of Students in Section	35	35	35
Number of Students Present	33	14	35
No. of Students below 40%	11	8	9
Pass % (≥40%)	66.67%	42.85%	74.29%
Average Marks	12.43	11.5	34.8
Highest Marks Obtained	28	24	67

(Subject Teacher)
Mr. Praveen Kumar

(HoD/ECE)
Prof. (Dr.) R.P.S Chauhan 02/12/19

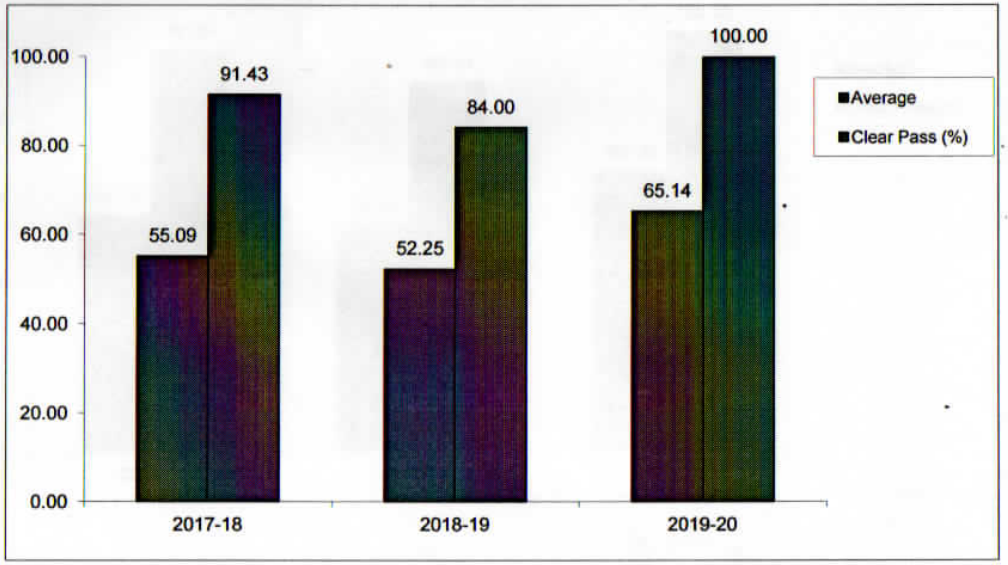
...S ENGINEERING COLLEGE, GHAZIA...D

Department of Electronics & Communication Engineering

Result Analysis for EC1 3rd Year Even Semester 2019-20

Subject Name	Subject Code	Session: 2017-18				Session: 2018-19				Session: 2019-20					Avg Diff. wrt 2017-18	Avg Diff. wrt 2018-19
		Students	Average	Pass %	CP	Students	Average	Pass %	CP	Students	Result Declared	Average	Pass %	CP		
INDUSTRIAL MANAGEMENT	RAS 601	35	58.74	100	0	50	55.94	100	0	35	35	66.29	100	0	7.55	10.35
CYBER SECURITY	RUC 601	N.A.				50	54.83	100	0	35	35	65.59	100	0	N.A.	10.76
CONTROL SYSTEM 1	RIC 603	35	56.89	100	0	50	49.34	90	5	35	35	66.29	100	0	9.40	16.95
MICROWAVE ENGINEERING	REC 601	35	51.86	97.14	1	50	52.37	98	1	35	35	65.80	100	0	13.94	13.43
DIGITAL COMMUNICATION	REC 602	35	50.40	97.14	1	50	52.06	90	5	35	35	60.45	100	0	10.05	8.39
ADVANCE DIGITAL DESIGN USING VERILOG	REC 064	35	58.74	100	0	50	48.97	92	4	22	22	65.00	100	0	6.26	16.03
RADAR ENGINEERING	REC 065	N.A.				N.A.				13	13	68.79	100	0	N.A.	N.A.
Overall Pass%		91.43				84				100					100.00	16.00
Class Average		55.09				52.25				65.14					65.14	12.89

Subject Name	Code	Faculty Name
INDUSTRIAL MANAGEMENT	RAS 601	Prof. Sunil Kr Pandey (ME)
CYBER SECURITY	RUC 601	Prof. Sameer Anand (EN)
CONTROL SYSTEM 1	RIC 603	Prof. Myurika Saxena
MICROWAVE ENGINEERING	REC 601	Prof. Praveen Chourasia
DIGITAL COMMUNICATION	REC 602	Prof. Balwant Singh
ADVANCE DIGITAL DESIGN USING VERILOG	REC 064	Prof. Pankaj Goel
RADAR ENGINEERING	REC 065	Prof. Arjun Singh Katiyar



(HOD, ECE) 05/08/2020

S ENGINEERING COLLEGE, GHAZIAB D

Department of Electronics & Communication Engineering

Result Analysis for EC2 3rd Year Even Semester 2019-20

Subject Name	Subject Code	Session: 2017-18				Session: 2018-19				Session: 2019-20					Avg Diff. wrt 2017-18	Avg Diff. wrt 2018-19
		Students	Average	Pass %	CP	Students	Average	Pass %	CP	Students	Result Declared	Average	Pass %	CP		
INDUSTRIAL MANAGEMENT	RAS 601	46	58.22	100	0	50	57.06	100	0	36	36	66.51	100	0	8.29	9.45
CYBER SECURITY	RUC 601	N.A.				50	58.97	100	0	36	36	66.03	100	0	N.A.	7.06
CONTROL SYSTEM 1	RIC 603	46	56.89	100	0	50	54.57	100	0	36	36	66.27	100	0	9.38	11.70
MICROWAVE ENGINEERING	REC 601	46	56.04	100	0	50	51.37	94	3	36	36	66.11	100	0	10.07	14.74
DIGITAL COMMUNICATION	REC 602	46	54.22	97.82	1	50	50.31	94	3	36	36	66.51	100	0	12.29	16.20
ADVANCE DIGITAL DESIGN USING VERILOG	REC 064	46	60.56	100	0	50	48.74	96	2	23	23	67.08	100	0	6.52	18.34
RADAR ENGINEERING	REC 065	N.A.				N.A.				13	13	64.84	100	0	N.A.	N.A.
Overall Pass%		95.65				88				100.00					4.35	12.00
Class Average		56.24				53.50				66.28					10.04	12.78

Subject Name	Code	Faculty Name
INDUSTRIAL MANAGEMENT	RAS 601	Prof. Sunil Kr Pandey (ME)
CYBER SECURITY	RUC 601	Prof. Sameer Anand (EN)
CONTROL SYSTEM 1	RIC 603	Prof. Praveen Kumar
MICROWAVE ENGINEERING	REC 601	Prof. Praveen Chourasia
DIGITAL COMMUNICATION	REC 602	Prof. Balwant Singh
ADVANCE DIGITAL DESIGN USING VERILOG	REC 064	Prof. Pankaj Goel
RADAR ENGINEERING	REC 065	Prof. Arjun Singh Katiyar

(HOD, ECE) 05/08/2020