IMS ENGINEERING COLLEGE GHAZIABAD
(YEAR OF ESTABLISHMENT – 2002)
[Approved by AICTE & Affiliated to AKTU, Lucknow]

Supporting Document

2.5.2 Mechanism to deal with internal/external examination related grievances is transparent, time- bound and efficient

IMS ENGINEERING COLLEGE,GZB		
Sessional Question Paper	IMSEC/QF/49	
	Page 1 of 1	
	Issue no: 02	
	Issue date: 1 May 2010	
1st Sessional Examination (CT-1), Odd Sem. 2019-20		
Subject Name: Integrated Circuits	Subject code	REC 501
Roll No. of student	Max Marks	30
	Max time	1:30hrs
For EC1, EC2 3rd Year	Approved By Director	

Note: Attempt any ***six*** questions (6×5=30)

Q.1 What are the desirable characteristics of current mirror circuit? Draw the simple BJT current mirror circuit and derive the expression of current transfer ratio.

Q.2 For V_{dd} = 1.8V and using I_{REF} = 50μA. It is required to design the circuit of Fig.1 to obtain an output current whose nominal value is 50μA. Find R if Q_1 and Q_2 are matched with channel lengths of 0.5μm, channel widths of 5μm, V_t = 0.5V and k_n' = 250μA/V². What is the lowest possible value of V_o? Assuming that for this process technology the early voltage V'_A = 20V/μm, find the output resistance of current source.

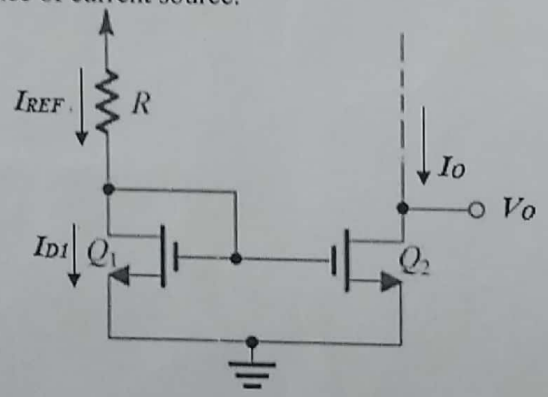


Fig.1

Q.3 Explain Wilson Current mirror. How the V_{DS} mismatching is avoided by improved Wilson mirror?

Q.4 Draw the circuit diagram of cascode current mirror; also write the advantage and disadvantage of cascode current mirror.

Q.5 Design a CMOS full adder circuit with inputs A, B, C and two output S and C_0.

Q.6 Sketch the CMOS realization of the following Boolean function-

(a) $Y = \overline{(A+B+C).D}$ (b) $Y = \bar{A}B + A\bar{B}$

Q.7 Sketch the CMOS implementation of SR flip-flop and explain its working.

Q.8 Draw the D-flip flop using CMOS. Also draw and explain its master slave configuration.

For office use only					
Course Outcomes and Question mapping matrix					
CO1	CO2	CO3	CO4	CO5	CO6
Q. 1, 2, 3, 4	-	Q. 5, 6, 7, 8	-	-	-

Chandra
30/08/19

IMSENGINEERINGCOLLEGE,GZB		
Sessional Question Paper	IMSEC/QF/49	
	Page 1 of 1	
	Issue no: 02	
	Issue date:1 May 2010	
2nd Sessional Examination (CT-2), Odd Sem. 2019-20		
Subject Name: Integrated Circuits	Subject code	REC 501
Roll No. of student	Max Marks	30
	Max time	1:30hrs
For EC1, EC2 3rd Year	Approved By Director	

Note: Attempt any ***six*** questions (6×5=30)

Q.1 Draw the generalized impedance converter and derive its impedance equation. Also simulate an Inductor.

Q.2 Explain how a Schmitt Trigger circuit works with a neat diagram. Design a Schmitt trigger with V_{UT} = 2V, V_{LT} = -2V. Assume ± V_{sat} = ±13V.

Q.3 Draw the circuit of Sallen Key filter and derive the expression of its transfer function. Also design the equal component Sallen key high pass filter.

Q.4 Derive the expression of voltage gain in KHN biquad filter. Draw the KHN biquad filter and drive transfer function of the BPF and LPF from that.

Q.5 Draw and explain basic logarithmic amplifier. Also explain temperature compensated logarithmic amplifier.

Q.6 Explain the working of precision full wave rectifier with necessary waveform.

Q.7 Design a wide band pass filter with f_l = 500Hz, f_h = 1500Hz and a pass band gain of 4. Draw frequency response of band pass filter and find value of Q.

Q.8 Design a 2nd order low pass Butterworth filter with cut off frequency of 1 KHz.

For office use only					
Course Outcomes and Question mapping matrix					
CO1	CO2	CO3	CO4	CO5	CO6
-	Q. 3, 4, 7, 8	-	Q.2, 5, 6	-	Q.1

07/11/19

IMSENGINEERINGCOLLEGE,GZB		
Sessional Question Paper	IMSEC/QF/49	
	Page 1 of 1	
	Issue no: 02	
	Issue date:1 May 2010	
PUT Examination, Odd Sem. 2019-20		
Subject Name: Integrated Circuits	Subject code	REC 501
Roll No. of student	Max Marks	70
	Max time	3 Hrs
Prepared By: MR	Approved By Director	

Note: All sections are compulsory. If require any missing data; then choose suitably.

Section-A

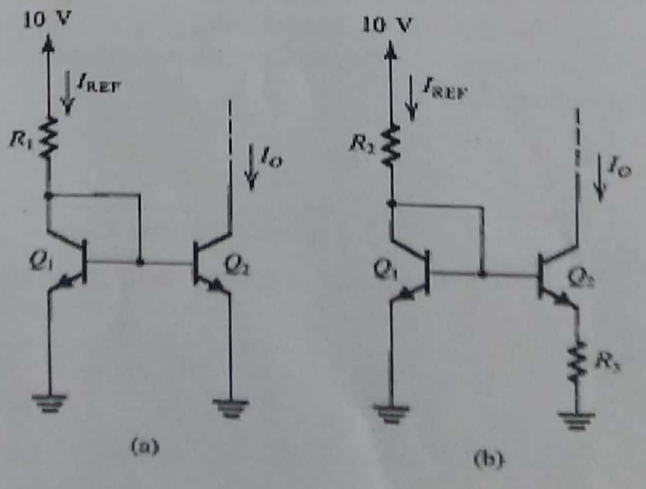
Q.1 Attempt any **seven** parts of this question (2×7=14)

a) What is the advantage of Widlar current source over simple constant current source?
b) Define and give significance of Slew Rate.
c) Write the advantage of active filter over passive filter?
d) What do you mean by a frequency response of a filter circuit?
e) Why CMOS NAND is preferred over CMOS NOR?
f) Give two application of analog multiplier.
g) What is a Super Diode?
h) List the application of PLL.
i) The basic step of a 8-bit DAC is 20mV. If 00000000 represents 0V, what is represented by the input 10110111.
j) What are the advantages of CMOS logic family?

Section-B

Attempt any ***three*** questions of this section. (7×3=21)

Q.2 Explain Widlar current source.
Following Fig. (a) and (b) shows the two circuit for generating a constant current of 10μA which operates from 10V supply. Determine the value of required resistors assuming that V_{BE} = 0.7V at a current of 1mA and neglecting the effect of finite β.



22/11/19

Q.3 Draw the CMOS realization of the following Boolean expression
(i) $Y = \overline{A + B(C + D)}$ (ii) $Y = \overline{(A + B).C + D}$

Q.4 Explain the circuit of following current mirror and also discuss their advantage-
(i) Wilson current mirror (ii) Base current compensated current mirror

Q.5 Explain the following circuit using op-amp
(i) Schmitt trigger (ii) Comparator and zero crossing detector

Q.6 (i) Design a wide band pass filter with f_L = 200Hz, f_H =1KHz and a pass band gain of 4.
(ii) Design a 2nd order Butterworth high pass filter with cut-off frequency of 1KHz.

Q.7 Explain R-2R ladder type digital to analog converter.

Section-C

Attempt ***any one part*** of each questions of this section. (7×5=35)

Q.8 a) Discuss the frequency response of 741opamp. Relate unity-gain bandwidth and slew rate.
b) How the short circuit protection is achieved in the output stage of 741 op-amp?
c) Explain MOSFET current mirror, also show the effect of V_o on I_o.

Q.9 a) Draw the circuit of KHN biquad filter and derive the expression of its voltage gain
b) Realize generalized impedance converter (GIC) with op-amp. How the inductor is simulated using this GIC.
c) Implementation the following filter using op-amp
(i) Notch filter (ii) Narrow band pass filter

Q.10 a) Design a CMOS full adder circuit with three inputs A, B, C and two output S and C_o.
b) Give the CMOS implementation of clocked SR flip-flop and explain its working.
c) Draw the D-flip flop using CMOS. Also draw and explain its master slave configuration.

Q.11 a) Draw and explain the circuit of temperature compensated logarithmic amplifier.
b) Explain working of precision full wave rectifier with necessary waveform.
c) Draw and explain the circuit of square wave generator (astable multivibrator) using op-amp and derive the expression of output frequency.

Q.12 a) Explain the operation of dual slope ADC.
b) Draw and explain the circuit of astable multivibrator using 555 timer. Also derive the expression of frequency and duty cycle of output wave form.
c) Draw the block diagram of a PLL and explain its operation. Explain lock-in-range, capture range and pull-in time of a PLL.

For office use only					
Course Outcomes and Question mapping matrix					
CO1	CO2	CO3	CO4	CO5	CO6
Q.1(a,b), Q.2, Q.4, Q.8	Q.1(c,d), Q.6, Q.9	Q.1(e,j), Q.3, Q.10	Q.1(f, g), Q.5, Q.11	Q.1(i), Q.7, Q.12 (a,c)	Q.1(h), Q.12(b)

IMS ENGINEERING COLLEGE, Ghaziabad	IMSEC/QF/59
Schedule of Examination	Page 1 of 1
	Issue No: 01
Sessional Test-I (Odd Semester 2019-20)	Issue Date: 08/10/08
Prepared by: MR	Approved by: Director

Year/ (Sem)	BRANCH	02-09-2019	03-09-2019	04-09-2019	05-09-2019	06-09-2019	07-09-2019
		02:30pm-04:00 pm	02:30pm-04:00 pm	02:30pm-04:00 pm	02:30pm-04:00 pm	02:30pm-04:00 pm	02:30pm-04:00 pm
2nd YEAR/3rd Sem	EN	Maths IV (KAS302)	Basic Signals & Systems (KEE-303)		Electromagnetic Field Theory (KEE-301)	Electrical Measurements & Instrumentation (KEE-302)	Technical Communication (KAS301)
3rd year /5th Sem	EN	Electrical Machines -II (REE-501)	Managerial Economics (RAS 501)	Control System (REE-503)	Principles of Communication (REE-052)	Power Transmission & Distribution (REE-502)	Sociology (RAS502)
4th YEAR/7th Sem	EN	Power System Protection (REE-702)	Communication Systems (REN-701)	Telemetry & Data Transmission (REN-075)	Utilization of Electrical Energy & Electric Traction (REE-071)		

Note 1: Student entry will not be allowed after commencment of exam.

2: Students are not allowed to leave examination hall before completion of exam.

Annu 28/8/19

Mrs. Annu Govind
HOD EN

IMS ENGINEERING COLLEGE, Ghaziabad	IMSEC/QF/59
Schedule of Examination	Page 1 of 1
	Issue No: 01
Sessional Test-II (Even Sem 2018-19)	Issue Date: 08/10/08
Prepared by: MR	Approved by: Director

Year/ (Sem)	BRANCH	01-04-2019 (Mon)	06-04-2019 (Sat)	08-04-2019 (Mon)	13-04-2019 (Sat)	15-04-2019 (Mon)	20-04-2019 (Sat)
		9:00 am - 10:30 am	3:00pm - 4:30 pm	9:00 am - 10:30 am	3:00pm - 4:30 pm	9:00 am - 10:30 am	3:00 pm - 4:30 pm
2nd YEAR/4th Sem	EN	EMFT (REC-402)	Power Plant Engg. (REE-401)	Electrical Machines-I (REE-402)	Material Science (ROE-047)	Network Analysis & Synthesis (REE-405)	Environment & Ecology (RAS-402)
3rd year /6th Sem	EN	Special Electrical Machine (REE-064)	Cyber Security (RUC 601)	Power System Analysis (REE-603)	Micro Processor (REE-602)	Power Electronics (REE-601)	Industrial Management (RAS-601)

Note 1: Student entry will not be allowed after commencment of exam.

2: Students are not allowed to leave examination hall before completion of exam.

26/03/2019

Prof. R. K. Chauhan
HOD EN

IMS ENGINEERING COLLEGE, Ghaziabad	IMSEC/QF/59
Schedule of Examination	Page 1 of 1
	Issue No: 01
Pre University Test (Odd Semester.2019-20)	Issue Date: 08/10/08
Prepared by: MR	Approved by: Director

Year/ (Sem)	BRANCH	25-11-2019 (Mon) 01:30pm-04:30 pm	26-11-2019 (Tues) 01:30pm-04:30 pm	27-11-2019 (Wed) 01:30pm-04:30 pm	28-11-2019 (Thur) 01:30pm-04:30 pm	29-11-2019 (Fri) 01:30pm-04:30 pm	30-11-2019 (Sat) 01:30pm-04:30 pm
2nd YEAR/3rd Sem	EN	Maths IV (KAS 302)	Technical Communication (KAS301)	Electrical Measurements & Instrumentation (KEE-302)		Electromegnetic Field Theory (KEE 301)	Basic Signals & Systems (KEE-303)
3rd year /5th Sem	EN	Control System (REE-503)	Managerial Economics (RAS 501)	Electrical Machines -II (REE-501)	Power Transmission & Distribution (REE-502)	Principles of Communication (REE-052)	Sociology (RAS502)
4th YEAR/7th Sem	EN	Understanding the Human Being Comprehensively Human Aspiration Audits Fulfilment (ROE074)	Power System Protection (REE-702)	Utilization of Electrical Energy & Electric Traction (REE-071)	Telemetry & Data Transmission (REN-075)	Communication Systems (REN-701)	

Note 1: Student entry will not be allowed after commencment of exam.

2: Students are not allowed to leave examination hall before completion of exam.

Annu 18/11/19

Mrs. Annu Govind

HOD-EN

IMS ENGINEERING COLLEGE, Ghaziabad	IMSEC/QF/59
Schedule of Examination	Page 1 of 1
	Issue No: 01
Pre University Test (Odd Semester.2019-20)	Issue Date: 08/10/08
Prepared by: MR	Approved by: Director

Year/ (Sem)	BRANCH	25-11-2019 (Mon) 01:30pm-04:30 pm	26-11-2019 (Tues) 01:30pm-04:30 pm	27-11-2019 (Wed) 01:30pm-04:30 pm	28-11-2019 (Thur) 01:30pm-04:30 pm	29-11-2019 (Fri) 01:30pm-04:30 pm	30-11-2019 (Sat) 01:30pm-04:30 pm
2nd YEAR/3rd Sem	EN	Maths IV (KAS 302)	Technical Communication (KAS301)	Electrical Measurements & Instrumentation (KEE-302)		Electromegnetic Field Theory (KEE 301)	Basic Signals & Systems (KEE-303)
3rd year /5th Sem	EN	Control System (REE-503)	Managerial Economics (RAS 501)	Electrical Machines -II (REE-501)	Power Transmission & Distribution (REE-502)	Principles of Communication (REE-052)	Sociology (RAS502)
4th YEAR/7th Sem	EN	Understanding the Human Being Comprehensively Human Aspiration Audits Fulfilment (ROE074)	Power System Protection (REE-702)	Utilization of Electrical Energy & Electric Traction (REE-071)	Telemetry & Data Transmission (REN-075)	Communication Systems (REN-701)	

Note 1: Student entry will not be allowed after commencment of exam.

2: Students are not allowed to leave examination hall before completion of exam.

Annu 18/11/19

Mrs. Annu Govind

HOD-EN

Department of Computer Science & Engineering
IMS Engineering College, Ghaziabad
Room# C-101 (02-12-2020 to 08-12-2020) (09:00 AM TO 10:30 AM)

I	II	III	IV	V	VI	VII	VIII	IX	X
2nd yr CS1			**2nd yr CS1**				**2nd yr CS1**		
1901430120001			**1901430120009**			**1901430120016**			**1901430120024**
1901430120002			**1901430120010**			**1901430120017**			**1901430120025**
1901430120003			**1901430120012**			**1901430120019**			**1901430120026**
1901430120004			**1901430120013**			**1901430120021**			**1901430120027**
1901430120007			**1901430120014**			**1901430120022**			**1901430120028**
1901430120008			**1901430120015**			**1901430120023**			**1901430120029**

2nd Yr. CS1:1901430120001 to 1901430120029

Total: 24

Department of Computer Science & Engineering
IMS Engineering College, Ghaziabad
Room# C-102 (02-12-2020 to 08-12-2020) (09:00 AM TO 10:30 AM)

I	II	III	IV	V	VI	VII	VIII	IX	X
2nd yr CS1			**2nd yr CS1**				**2nd yr CS1**		
1901430120030			**1901430120037**			**1901430120043**			**1901430120049**
1901430120031			**1901430120038**			**1901430120044**			**1901430120050**
1901430120032			**1901430120039**			**1901430120045**			**1901430120051**
1901430120033			**1901430120040**			**1901430120046**			**1901430120052**
1901430120034			**1901430120041**			**1901430120047**			**1901430120053**
1901430120035			**1901430120042**			**1901430120048**			**1901430120054**
1901430120036									**1901430120055**

2nd Yr. CS1: 1901430120030 to 1901430120055 26

Total: 26

Department of Computer Science & Engineering
IMS Engineering College, Ghaziabad
Room# C-103 (02-12-2020 to 08-12-2020) (09:00 AM TO 10:30 AM)

I	II	III	IV	V	VI	VII	VIII	IX	X
2nd yr CS1			**2nd yr CSE1**				**2nd yr CSE1**		
1901430120056			**1901430100001**			**1901430100007**			**1901430100013**
1901430120058			**1901430100002**			**1901430100008**			**1901430100014**
1901430120059			**1901430100003**			**1901430100009**			**1901430100015**
1901430120060			**1901430100004**			**1901430100010**			**1901430100016**
1901430120061			**1901430100005**			**1901430100011**			**1901430100017**
1901430120062			**1901430100006**			**1901430100012**			**1901430100018**
1901430120063									**1901430100019**

2nd Yr. CS1: 190143120056 to 1901430120063 07

2nd Yr. CSE1: 19014310100001 to 1901430100019 19

Total: 26

Department of Computer Science & Engineering
IMS Engineering College, Ghaziabad
Room# C-104 (02-12-2020 to 08-12-2020) (09:00 AM TO 10:30 AM)

I	II	III	IV	V	VI	VII	VIII	IX	X
2nd yr CSE1			**2nd yr CSE1**				**2nd yr CSE1**		
1901430100020			**1901430100027**			**1901430100033**			**1901430100039**
1901430100021			**1901430100028**			**1901430100034**			**1901430100040**
1901430100022			**1901430100029**			**1901430100035**			**1901430100041**
1901430100023			**1901430100030**			**1901430100036**			**1901430100042**
1901430100024			**1901430100031**			**1901430100037**			**1901430100043**
1901430100025			**1901430100032**			**1901430100038**			**1901430100044**
1901430100026									**1901430100045**

2nd Yr. CSE1: 1901430100020 to 1901430100045 26

Total: 26

Department of Computer Science & Engineering
IMS Engineering College, Ghaziabad
Room# C-105 (02-12-2020 to 08-12-2020) (09:00 AM TO 10:30 AM)

I	II	III	IV	V	VI	VII	VIII	IX	X
2nd yr CSE1			**2nd yr CSE1/CSE2**				**2nd yr CSE2**		
1901430100046			**1901430100054**			**1901430100060**			**1901430100063**
1901430100047			**1901430100055**			**1901430100061**			**1901430100065**
1901430100048			**1901430100056**			**1901430100062**			**1901430100066**
1901430100049			**1901430100057**			**1901430120006**			**1901430100067**
1901430100051			**1901430100058**			**UTKARSH GUPTA**			**1901430100068**
1901430100052			**1901430100059**			**1901430100064**			**1901430100069**
1901430100053									**1901430100070**

2nd Yr. CSE1: 1901430100046 to 1901430100062, 1901430120006, UTKARSH GUPTA 18

2nd Yr. CSE2: 1901430100064 to 19014301000070 08

Total: 26

Department of Computer Science & Engineering
IMS Engineering College, Ghaziabad
Room# C-106 (02-12-2020 to 08-12-2020) (09:00 AM TO 10:30 AM)

I	II	III	IV	V	VI	VII	VIII	IX	X
2nd yr CSE2			**2nd yr CSE2**				**2nd yr CSE2**		
1901430100071			**1901430100078**			**1901430100084**			**1901430100090**
1901430100072			**1901430100079**			**1901430100085**			**1901430100091**
1901430100073			**1901430100080**			**1901430100087**			**1901430100092**
1901430100074			**1901430100081**			**1901430100086**			**1901430100093**
1901430100075			**1901430100082**			**1901430100088**			**1901430100094**
1901430100076			**1901430100083**			**1901430100089**			**1901430100095**
1901430100077									**1901430100096**

2nd Yr. CSE2: 1901430100071 to 19014301000096 26

Total: 26

Department of Computer Science & Engineering
IMS Engineering College, Ghaziabad
Room# C-107 (02-12-2020 to 08-12-2020) (09:00 AM TO 10:30 AM)

I	II	III	IV	V	VI	VII	VIII	IX	X
2nd yr CSE2			**2nd yr CSE2**				**2nd yr CSE2**		
1901430100097			**1901430100105**			**1901430100111**			**1901430100117**
1901430100098			**1901430100106**			**1901430100112**			**1901430100118**
1901430100099			**1901430100107**			**1901430100113**			**1901430100120**
1901430100100			**1901430100108**			**1901430100114**			**1901430100121**
1901430100101			**1901430100109**			**1901430100115**			**1901430100122**
1901430100103			**1901430100110**			**1901430100116**			**1901430100123**
1901430100104									**1901430100124**

2nd Yr. CSE2: 1901430100097 to 19014301000124 26

Total: 26

Department of Computer Science & Engineering
IMS Engineering College, Ghaziabad
Room# C-108 (02-12-2020 to 08-12-2020) (09:00 AM TO 10:30 AM)

I	II	III	IV	V	VI	VII	VIII	IX	X
2nd yr CSE2/CSE3			**2nd yr CSE3**				**2nd yr CSE3**		
1901430120005			**1901430100129**			**1901430100135**			**1901430100141**
Amrendra Mohan Shukla			**1901430100130**			**1901430100136**			**1901430100142**
ADARSH KUMAR SINGH			**1901430100131**			**1901430100137**			**1901430100143**
1901430100125			**1901430100132**			**1901430100138**			**1901430100144**
1901430100126			**1901430100133**			**1901430100139**			**1901430100145**
1901430100127			**1901430100134**			**1901430100140**			**1901430100146**
1901430100128									**1901430100147**

2nd Yr. CSE2: 1901430120005 , Amrendra, Adarsh 03

2nd Yr. CSE3: 1901430100125 to 19014301000147 23

Total: 26

Department of Computer Science & Engineering
IMS Engineering College, Ghaziabad
Room# C-201 (02-12-2020 to 08-12-2020) (09:00 AM TO 10:30 AM)

I	II	III	IV	V	VI	VII	VIII	IX	X
2nd yr CSE3			**2nd yr CSE3**				**2nd yr CSE3**		
1901430100148			**1901430100156**			**1901430100162**			**1901430100168**
1901430100149			**1901430100157**			**1901430100163**			**1901430100169**
1901430100150			**1901430100158**			**1901430100164**			**1901430100170**
1901430100151			**1901430100159**			**1901430100165**			**1901430100171**
1901430100152			**1901430100160**			**1901430100166**			**1901430100172**
1901430100153			**1901430100161**			**1901430100167**			**1901430100173**
1901430100154									**1901430100174**

2nd Yr. CSE3: 1901430100148 to 19014301000174 26

Total: 26

Department of Computer Science & Engineering
IMS Engineering College, Ghaziabad
Room# C-202 (02-12-2020 to 08-12-2020) (09:00 AM TO 10:30 AM)

I	II	III	IV	V	VI	VII	VIII	IX	X
2nd yr CSE3/CSE4			**2nd yr CSE3/CSE4**				**2nd yr CSE4**		
1901430100175			**1901430100182**			**TRIPTI PANDEY**			**1901430100191**
1901430100176			**1901430100183**			**1901430100186**			**1901430100192**
1901430100177			**1901430100184**			**1901430100187**			**1901430100193**
1901430100178			**1901430100185**			**1901430100188**			**1901430100194**
1901430100179			**1901430120011**			**1901430100189**			**1901430100195**
1901430100180			**LUCKY RAM**			**1901430100190**			**1901430100196**
1901430100181									**1901430100197**

2nd Yr. CSE3: 1901430100175 to 19014301000185, **1901430120011 , Lucky Tripti** 14

2nd Yr. CSE4: 1901430100186 to 19014301000197 12

Total: 26

Department of Computer Science & Engineering
IMS Engineering College, Ghaziabad
Room# C-203 (02-12-2020 to 08-12-2020) (09:00 AM TO 10:30 AM)

I	II	III	IV	V	VI	VII	VIII	IX	X
2nd yr CSE4			**2nd yr CSE4**				**2nd yr CSE4**		
1901430100198			**1901430100205**			**1901430100211**			**1901430100217**
1901430100199			**1901430100206**			**1901430100212**			**1901430100218**
1901430100200			**1901430100207**			**1901430100213**			**1901430100219**
1901430100201			**1901430100208**			**1901430100214**			**1901430100220**
1901430100202			**1901430100209**			**1901430100215**			**1901430100221**
1901430100203			**1901430100210**			**1901430100216**			**1901430100222**
1901430100204									**1901430100223**

2nd Yr. CSE4: 1901430100198 to 19014301000223 26

Total: 26

Department of Computer Science & Engineering
IMS Engineering College, Ghaziabad
Room# C-204 (02-12-2020 to 08-12-2020) (09:00 AM TO 10:30 AM)

I	II	III	IV	V	VI	VII	VIII	IX	X
2nd yr CSE4			**2nd yr CSE4**				**2nd yr CSE4**		
1901430100224			**1901430100231**			**1901430100237**			**1901430100243**
1901430100225			**1901430100232**			**1901430100238**			**1901430100244**
1901430100226			**1901430100233**			**1901430100239**			**1901430100245**
1901430100227			**1901430100234**			**1901430100240**			**1901430130036**
1901430100228			**1901430100235**			**1901430100241**			**Ankit Kumar Verma**
1901430100229			**1901430100236**			**1901430100242**			
1901430100230									

2nd Yr. CSE4: 1901430100224 to 19014301000245,036,Ankit 24

Total: 24

IMS ENGINEERING COLLEGE, GHAZIABAD
ELECTRICAL & ELECTRONICS ENGG. DEPARTMENT
Result Analysis of EN, 3rd yr
SUBJECT- POWER SYSTEM-I (KEE501)

Sr. No	Roll No	Name	CT-1 (30)	CT-2 (30)	TEST-3 (100)
1	1814321001	AADARSH KUSHWAHA	6	13	57
2	1814321002	AAKASH SINGH	A	24	76
3	1814321003	AAKRITI MITTAL	A	27	72
4	1814321004	ABHISHEK	A	24	70
5	1814321005	ACHINT JINDAL	A	25	76
6	1814321006	AISHWARYA ARORA	A	28	74
7	1814321007	AKASH KUSHWAH	A	26	72
8	1814321008	AKHIL BHATIA	7	Absent	77
9	1814321009	AMAN DEEP SINGH	A	16	72
10	1814321010	ANKIT KUMAR CHAURASIYA	A	20	67
11	1814321011	ASHIRWARD PANDEY	A	Absent	53
12	1814321012	DHARMENDRA KUMAR .	A	13	60
13	1814321013	DHRUV BHARADWAJ	A	26	70
14	1814321014	DHRUV RAWAT	A	25	59
15	1814321015	DIVYANSHU MISRA	A	22	77
16	1814321016	GHANESH SINGH	A	26	78
17	1814321017	HARIOM .	A	25	73
18	1814321018	HARSH PARASHAR	A	16	64
19	1814321019	HARSHIT KUMAR	8	20	69
20	1814321020	HEMANT KUMAR SINGH	A	18	43
21	1814321021	KAILASH PAL	6	12	53
22	1814321022	KISHAN KUMAR	A	20	59
23	1814321023	MANIK GAUR	A	21	47
24	1814321024	MANOJ YADAV	14	15	57
25	1814321025	MOHAMMAD JAHID	A	18	46
26	1814321026	MOHD ALBER SHAH KHAN	A	20	60
27	1814321027	PAWAN KASHYAP	0	12	30
28	1814321028	PRATHAM GUPTA	A	22	49
29	1814321029	PRIYAM CHANDRA	A	24	78
30	1814321030	PUSHPENDRA YADAV	A	23	68
31	1814321031	RIYA SINGH	A	27	63
32	1814321032	RUDRANSH CHAUDHARY	A	16	40
33	1814321033	SACHIN KUMAR YADAV	26	23	64
34	1814321034	SHIVAM RAJPUT	A	23	73
35	1814321035	SHIVAM MISHRA	15	19	61
36	1814321036	SHREYA SACHAN	A	24	75
37	1814321037	SHUBHAM DUBEY	20	25	77
38	1814321038	SIDHARTH KUMAR SINGH	A	18	56
39	1814321039	SURAJ PRAKASH	A	20	59
40	1814321041	VED PRAKASH KUMAR	A	22	77
41	1814321042	VIKRANT ANKOLA	A	10	59
42	1901430219001	SHIVAM GOEAL	A	17	53

Result Analysis	CT-1	CT-2	TEST-3
Number of Students in Section	42	42	42
Number of Students Present	9	40	42
Total Pass student	4	39	41
Pass %(≥40%)	44.40%	97.50%	97.61%
Average Marks	11.1	20.625	63.40
Highest Marks	26	28	78

10/02/21
Atul Kumar Kushwaha
(Subject Teacher)

11/02/21
Mr. Vijay Kumar
(HOD-EN)

IMS ENGINEERING COLLEGE	IMSEC/QF/48
FORMATS	Page 1 of 1 Issue No: 02
Tutorials/ Assignments/ Quizzes	Issue Date: 1 May 2010
Prepared by: MR	Approved by: Director

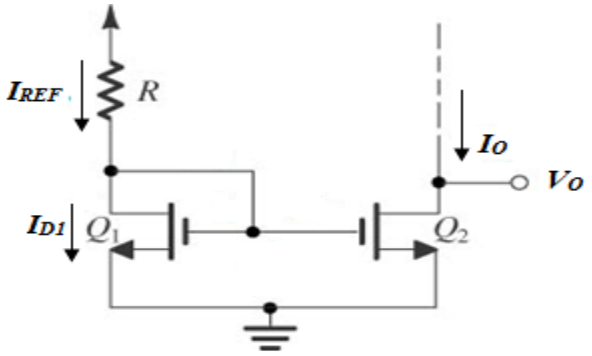
Subject Name : Integrated Circuits	Subject Code	REC-501
Date of Handout : 09-08-2019	Max Marks	
Date of Submission :14-08-2019		

ASSIGNMENT 1

Q.1. Explain MOSFET current mirror, also show the effect of V_o on I_o.

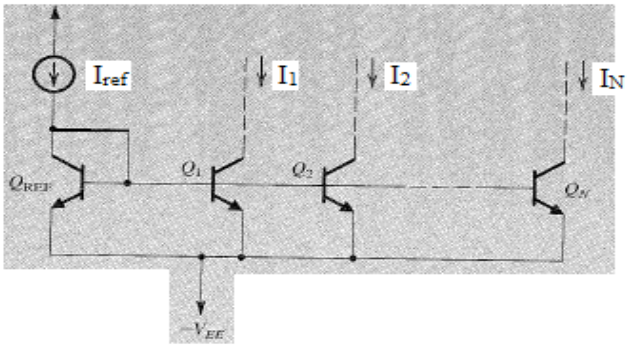
Q.2. Describe BJT current mirror and show the effect of finite β on the Current transfer ratio.

Q.3. For V_{dd} = 1.8V and using I_{REF} = 50µA. It is required to design the circuit of following fig. to obtain an output current whose nominal value is 50µA. Find R if Q_1 and Q_2 are matched with channel lengths of 0.5µm, channel widths of 5µm, V_t = 0.5V and k_n' = 250µA/V^2.What is the lowest possible value of V_o? Assuming that for this process technology the early voltage V'$_A$ = 20V/µm, find the output resistance of current source.



Q.4. Following Fig. shows an N output current mirror. Assuming that all transistors are matched and have finite β and ignoring the effect of finite output resistances, show that

$$I_1 = I_2 = \ldots I_N = \frac{Iref}{1+\frac{N+1}{\beta}}$$



For β = 100, find the maximum number of outputs for an error not exceeding 10%.

IMS ENGINEERING COLLEGE	IMSEC/QF/48
FORMATS	Page 1 of 1 Issue No: 02
Tutorials/ Assignments/ Quizzes	Issue Date: 1 May 2010
Prepared by: MR	Approved by: Director

Subject Name : IC	Subject Code	REC-501
Date of Handout : 16.08.2019	Max Marks	
Date of Submission : 23.08.2019		

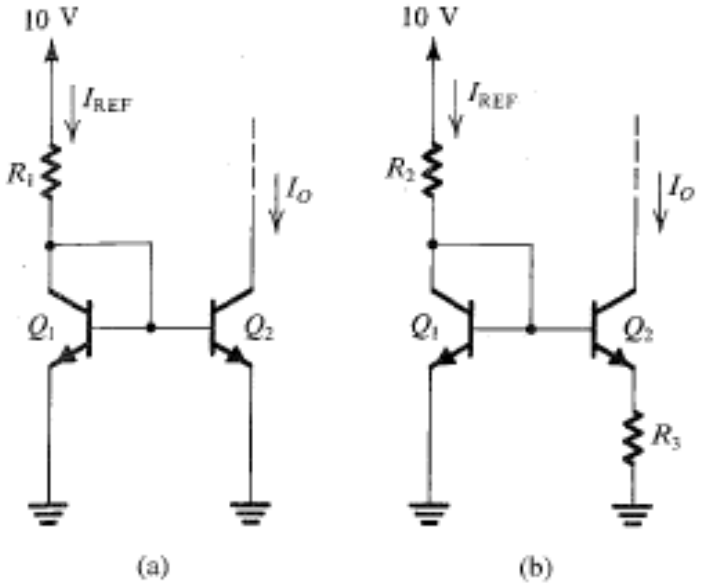
ASSIGNMENT 2

Q.1. Explain Wilson MOS mirror. Also draw the circuit of improved Wilson mirror.

Q.2. Draw the circuit of a bipolar mirror with base current compensation. Explain how it reduces the effect of β on current transfer ratio of current mirror.

Q.3. Explain the cascode current mirror. Write the advantage and disadvantage of the cascode current mirror.

Q.4. Explain Widlar current source.
Following figure (a) and (b) shows the two circuit for generating a constant current of 10μA which operates from 10V supply. Determine the value of required resistors assuming that V_{BE} = 0.7V at a current of 1mA and neglecting the effect of finite β.



(a) (b)

IMS ENGINEERING COLLEGE	IMSEC/QF/48
FORMATS	Page 1 of 1 Issue No: 02
Tutorials/ Assignments/ Quizzes	Issue Date: 1 May 2010
Prepared by: MR	Approved by: Director

Subject Name : Integrated Circuits	Subject Code	REC-501
Date of Handout : 30-09-2019	Max Marks	
Date of Submission : 09-09-2019		

ASSIGNMENT 3

Q.1 Draw the circuit diagram of CMOS inverter and explain its transfer characteristics.

Q.2 List the advantage of CMOS logic family

Q.3 Draw the CMOS realization of the following Boolean expression

a) $Y = \overline{A + B(C + D}$ b) $Y = \overline{(A + B).C + D}$

c) $Y = \overline{A + (B + C) + D.E}$ d) $Y = AB + \bar{A}\bar{B}$ e) $Y = AB + C$

Q.4 Discuss the features of CMOS circuit. Realize one AND-OR-INVERT (AOI) and one OR- AND-INVERT (OAI) function using CMOS logic circuit.

Q.5 Design a CMOS full adder circuit with three inputs A, B, C and two output S and C_o.

Q.6 Give a CMOS logic circuit that realizes the function of three input odd parity checker. Specificially, the output is to be high when an odd number (1 or 3) of the input are high. Attempt a design with 10 transistors (not counting those in the inverters) in each of the PUN and PDN.

IMS ENGINEERING COLLEGE	IMSEC/QF/48
FORMATS	Page 1 of 1 Issue No: 02
Tutorials/ Assignments/ Quizzes	Issue Date: 1 May 2010
Prepared by: MR	Approved by: Director

Subject Name : Integrated Circuit	Subject Code	REC-501
Date of Handout : 13-09-2019	Max Marks	
Date of Submission : 19-09-2019		

ASSIGNMENT 4

Q.1 For a process technology with L=0.5µm, n=1.5, p=6. Give size of all transistors in (i) a four input NOR and (ii) a four input NAND Gate. Also compare the area of two Gates and then shows that CMOS NAND is preferred over CMOS NOR.

Q.2 Determine the W/L ratios for all transistor used in CMOS implementation of the function $Y = \overline{A(B + CD)}$

Q.3 Give the CMOS implementation of clocked SR flip-flop and explain its working.

Q.4 Draw the D-flip flop using CMOS. Also draw and explain its master slave configuration.

IMS ENGINEERING COLLEGE	IMSEC/QF/48
FORMATS	Page 1 of 1 Issue No: 02
Tutorials/ Assignments/ Quizzes	Issue Date: 1 May 2010
Prepared by: MR	Approved by: Director

Subject Name : Integrated Circuit	Subject Code	REC-501
Date of Handout : 27-09-2019	Max Marks	
Date of Submission : 03-10-2019		

ASSIGNMENT 5

Q.1 Define the following term with reference to op-amp
(i) CMRR (ii) Slew rate (iii) PSRR
(iv) Input offset voltage (v) Bias current

Q.2 Realize generalized impedance converter (GIC) with op-amp. How the inductor is simulated using this GIC.

Q.3 Draw a second order low-pass and high pass filter and drive its transfer function. Design a second order low pass butterworth filter having upper cut-off frequency of 1kHz and a passband gain of 2

Q.4 Derive the expression of voltage gain in KHN biquad filter.

Q.5 Draw the following Circuit using op-amp
(i) Weighted Summer (ii) Difference Amplifier
(iii) V-I converter (iv) I-V Converter

IMS ENGINEERING COLLEGE	IMSEC/QF/48
FORMATS	Page 1 of 1 Issue No: 02
Tutorials/ Assignments/ Quizzes	Issue Date: 1 May 2010
Prepared by: MR	Approved by: Director

Subject Name : Integrated Circuit	Subject Code	REC-501
Date of Handout : 18-10-2019	Max Marks	
Date of Submission : 23-10-2019		

ASSIGNMENT 6

Q.1 Draw and explain the circuit of temperature compensated logarithmic amplifier.

Q.2 Draw and explain the circuit of temperature compensated anti-logarithmic amplifier.

Q.3 Draw and explain the circuit diagram of precision full wave rectifier.

Q.4 Explain inverting and non-inverting Schmitt trigger.

Q.4 Draw and explain the circuit of square wave generator circuit using op-amp.

IMS ENGINEERING COLLEGE	IMSEC/QF/48
FORMATS	Page 1 of 1 Issue No: 02
Tutorials/ Assignments/ Quizzes	Issue Date: 1 May 2010
Prepared by: MR	Approved by: Director

Subject Name : Integrated Circuit	Subject Code	REC-501
Date of Handout : 08-11-2019	Max Marks	
Date of Submission : 15-11-2019		

ASSIGNMENT 7

Q.1 Draw the functional block diagram of IC 555 and explain its working.

Q.2 Draw and explain monostable multivibrator using 555 timer and calculate its pulse width period.

Q.3 Draw and explain astable multivibrator using 555 timer and find the free running frequency of the output.

Q.4 An 8bit DAC has an input of 10011011 and 10V reference, find the corresponding output voltage.

Q.5 The basic step of a 8-bit DAC is 20mV. If 00000000 represents 0V, what is represented by the input 10110111.

Q.6 Explain the operation of Dual slope ADC.

(http://52.66.16.110/user)

- Dashboard (http://52.66.16.110/user#/dashboard)
- Module (http://52.66.16.110/user#/module_list)
- **Assignment**
  - Assignment
  - Student Wise Assignment Report
  - Faculty Wise Assignment Report
  - Section Wise Assignment Report

Assignment Report

Course	B.Tech	Stream	Electronics & Communication
Year	3 Year	Subject	Integrated Circuits (KEC 501)
Section	EC1		

#	Registered	Batch	Status	Roll No	Student Name	Assignment 07	Assignment 06	Assignment 05	Assignment 04	Assignment 03	Assignment 02	Assignment 01	Total
1	Yes	EC1	Regular	1714331042	RAHUL SINGH	1	0	1	1	1	1	1	6
2	Yes	EC1	Regular	1814331002	AASHI SINGH	1	1	0	1	1	1	1	6
3	Yes	EC1	Regular	1814331003	ABHISHEK KUMAR	1	1	1	1	1	1	1	7
4	Yes	EC1	Regular	1814331004	ABHISHEK KANDPAL	1	1	1	1	1	1	1	7
5	Yes	EC1	Regular	1814331005	ADITYA KUMAR	1	1	1	1	1	1	0	6
6	Yes	EC1	Regular	1814331006	ADITYA PANDEY	1	1	1	1	1	1	1	7
7	Yes	EC1	Regular	1814331007	AKHIL RUHELA	1	1	1	1	1	1	1	7
8	Yes	EC1	Regular	1814331008	AKSHAY VERMA	1	1	1	0	1	1	1	6
9	Yes	EC1	Regular	1814331009	ALI MAJAZ	1	1	1	1	1	1	1	7
10	Yes	EC1	Regular	1814331010	AMAN SAIFI	1	1	1	1	1	1	1	7
11	Yes	EC1	Regular	1814331011	ANIRUDH MANOJ	0	0	0	1	1	1	1	4
12	Yes	EC1	Regular	1814331012	ANMOL SHARMA	1	1	1	1	1	1	1	7
13	Yes	EC1	Regular	1814331013	ANSHUL SHARMA	1	1	1	1	1	1	1	7
14	Yes	EC1	Regular	1814331014	ANTRIKSH SAXENA	1	1	1	1	1	1	1	7
15	Yes	EC1	Regular	1814331015	ANUBHAV SINGH	1	1	1	1	1	1	1	7
16	Yes	EC1	Regular	1814331016	ARBAZ AKHTAR	1	1	1	1	1	1	1	7
17	Yes	EC1	Regular	1814331017	ARPIT SONI	1	1	1	1	1	1	1	7
18	Yes	EC1	Regular	1814331018	ASHISH CHAUDHARY	1	1	0	1	1	1	1	6
19	Yes	EC1	Regular	1814331019	ASHISH SHARMA	1	1	1	1	1	1	1	7
20	Yes	EC1	Regular	1814331020	AYUSH SAINI	0	1	0	0	1	1	1	4
21	Yes	EC1	Regular	1814331021	HARDIK RASTOGI	1	1	1	1	1	1	1	7
22	Yes	EC1	Regular	1814331022	HARSH JAISWAL	1	1	1	1	1	1	1	7
23	Yes	EC1	Regular	1814331023	JATIN AGARWAL	1	1	1	1	1	1	1	7
24	Yes	EC1	Regular	1814331024	JATIN RANA	1	1	1	1	1	1	1	7

(http://52.66.16.110/user)

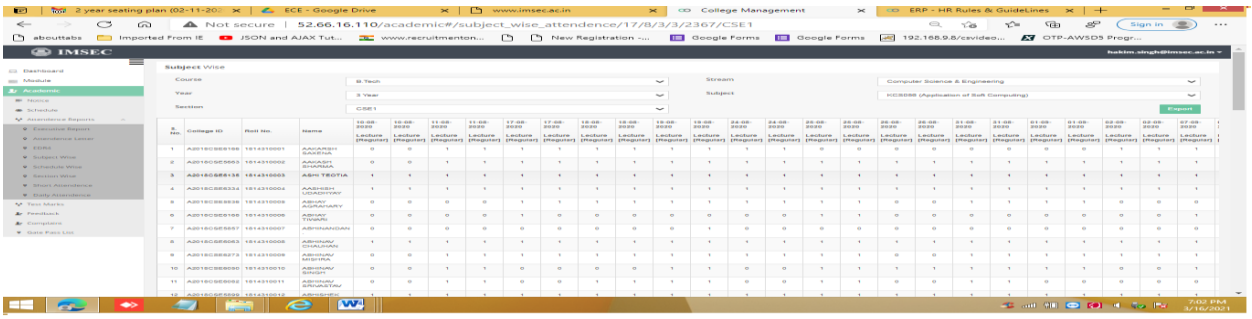
- Dashboard (http://52.66.16.110/user#/dashboard)
- Module (http://52.66.16.110/user#/module_list)
- **Assignment**
  - Assignment
  - Student Wise Assignment Report
  - Faculty Wise Assignment Report
  - Section Wise Assignment Report

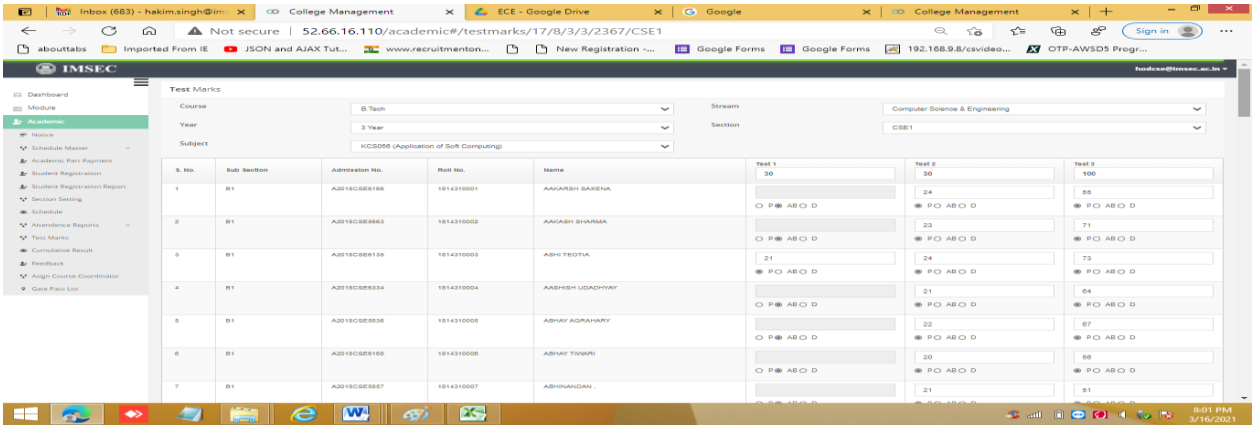
#	Registered	Batch	Status	Roll No	Student Name	Assignment 07	Assignment 06	Assignment 05	Assignment 04	Assignment 03	Assignment 02	Assignment 01	Total
25	Yes	EC1	Regular	1814331025	JAYA SINHA	1	1	1	1	1	1	1	7
26	Yes	EC1	Regular	1814331026	KRITIKA NATH	1	1	1	1	1	1	0	6
27	Yes	EC1	Regular	1814331027	MANSI SAXENA	1	1	1	1	1	1	1	7
28	Yes	EC1	Regular	1814331028	ARMAN SHAH	1	1	1	1	1	1	1	7
29	Yes	EC1	Regular	1814331029	MUDIT PRATAP SINGH	1	1	1	1	1	1	1	7
30	Yes	EC1	Regular	1814331030	MUKUL CHAUHAN	1	1	1	1	1	1	1	7
31	Yes	EC1	Regular	1814331031	MUNESH KUMAR SINGH	1	1	0	1	0	1	1	5
32	Yes	EC1	Regular	1814331032	MANIK CHOUDHARY	1	1	1	1	1	1	1	7
33	Yes	EC1	Regular	1814331033	NIKHIL KUMAR	0	1	1	1	1	1	1	6
34	Yes	EC1	Regular	1814331034	NISHA .	1	1	1	1	1	1	1	7
35	Yes	EC1	Regular	1814331035	NITESH UPADHYAY	1	1	1	1	1	1	1	7
36	Yes	EC1	Regular	1814331036	PRABHAT MITTAL	1	1	1	1	1	1	1	7
37	Yes	EC1	Regular	1814331037	PRADEEP DUBEY	1	1	1	1	1	1	1	7
38	Yes	EC1	Regular	1814331038	PRAKHAR TRIVEDI	1	0	0	0	1	1	0	3
39	Yes	EC1	Regular	1814331039	RACHIT GARG	1	1	1	1	1	1	1	7
40	Yes	EC1	Regular	1814331040	RISHABH GUPTA	1	0	1	1	1	1	1	6
41	Yes	EC1	Regular	1814331041	RIYA AGARWAL	1	1	1	1	1	1	1	7
42	Yes	EC1	Regular	1814331042	SAKSHI VARSHNEY	1	1	1	1	1	1	1	7
43	Yes	EC1	Regular	1814331043	SARANSH RAI	1	1	1	1	1	1	1	7
44	Yes	EC1	Regular	1814331044	SARTHAK GUPTA	1	1	1	1	1	1	1	7
45	Yes	EC1	Regular	1814331045	SAURABH GUPTA	1	1	1	1	1	1	1	7
46	Yes	EC1	Regular	1814331046	SHASHWAT DWIVEDI	0	1	1	1	1	1	1	6
47	Yes	EC1	Regular	1814331047	SHELENDRA RAGHAV	1	0	0	0	1	1	0	3
48	Yes	EC1	Regular	1814331048	SHIVAM KATIYAR	1	1	1	1	1	1	1	7
49	Yes	EC1	Regular	1814331049	SHIVANGI MISHRA	1	1	1	1	1	1	1	7
50	Yes	EC1	Regular	1814331050	SUPREET DEOL	1	1	1	1	1	1	1	7
51	Yes	EC1	Regular	1814331051	TANISH VARSHNEY	1	1	1	1	1	1	1	7
52	Yes	EC1	Regular	1814331052	TANISHKA VATS	1	1	1	1	1	1	1	7
53	Yes	EC1	Regular	1814331053	TUSHAR KUMAR	1	1	1	1	1	1	1	7
54	Yes	EC1	Regular	1814331054	UTKARSH SINGH	0	1	1	1	1	1	1	6
55	Yes	EC1	Regular	1814331055	VED PRAKASH SHARMA	1	1	1	1	1	1	1	7
56	Yes	EC1	Regular	1814331056	VISHAL RANA	1	1	1	1	1	1	1	7

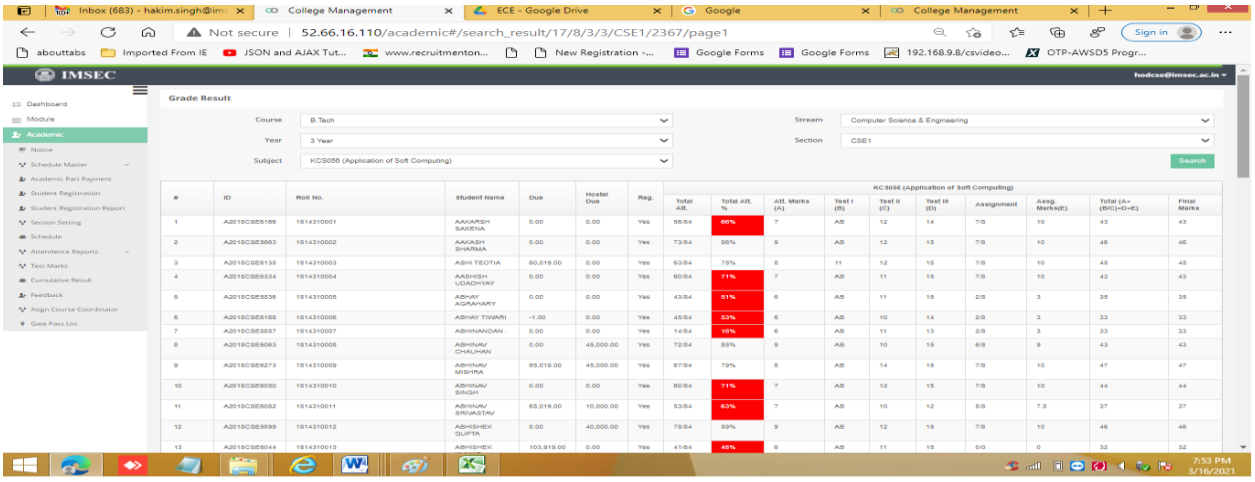
(http://52.66.16.110/user)

- Dashboard (http://52.66.16.110/user#/dashboard)
- Module (http://52.66.16.110/user#/module_list)
- **Assignment**
  - Assignment
  - Student Wise Assignment Report
  - Faculty Wise Assignment Report
  - Section Wise Assignment Report

#	Registered	Batch	Status	Roll No	Student Name	Assignment 07	Assignment 06	Assignment 05	Assignment 04	Assignment 03	Assignment 02	Assignment 01	Total
57	Yes	EC1	Regular	1814331057	YASH DIXIT	1	1	0	0	0	0	0	2
58	Yes	EC1	Regular	1814331058	YASHASVI SINGH	1	1	1	1	1	1	1	7


IMSEC
Subject Wise
Course
B.Tech
Year
3 Year
Section
CSE1
Stream
Computer Science & Engineering
Subject
KCS056 (Application of Soft Computing)


IMSEC
Test Marks
Course
B.Tech
Year
3 Year
Subject
KCS056 (Application of Soft Computing)
Stream
Computer Science & Engineering
Section
CSE1


IMSEC
Grade Result
Course
B.Tech
Year
3 Year
Subject
KCS056 (Application of Soft Computing)
Stream
Computer Science & Engineering
Section
CSE1
Search

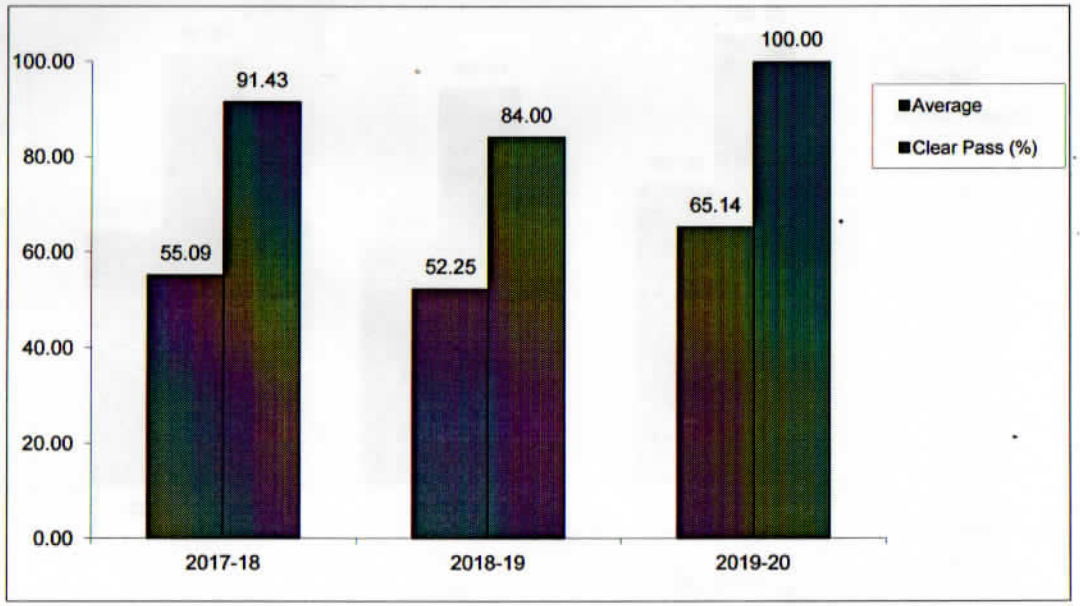
...S ENGINEERING COLLEGE, GHAZIA...D

Department of Electronics & Communication Engineering

Result Analysis for EC1 3rd Year Even Semester 2019-20

Subject Name	Subject Code	Session: 2017-18				Session: 2018-19				Session: 2019-20					Avg Diff. wrt 2017-18	Avg Diff. wrt 2018-19
		Students	Average	Pass %	CP	Students	Average	Pass %	CP	Students	Result Declared	Average	Pass %	CP		
INDUSTRIAL MANAGEMENT	RAS 601	35	58.74	100	0	50	55.94	100	0	35	35	66.29	100	0	7.55	10.35
CYBER SECURITY	RUC 601	N.A.				50	54.83	100	0	35	35	65.59	100	0	N.A.	10.76
CONTROL SYSTEM 1	RIC 603	35	56.89	100	0	50	49.34	90	5	35	35	66.29	100	0	9.40	16.95
MICROWAVE ENGINEERING	REC 601	35	51.86	97.14	1	50	52.37	98	1	35	35	65.80	100	0	13.94	13.43
DIGITAL COMMUNICATION	REC 602	35	50.40	97.14	1	50	52.06	90	5	35	35	60.45	100	0	10.05	8.39
ADVANCE DIGITAL DESIGN USING VERILOG	REC 064	35	58.74	100	0	50	48.97	92	4	22	22	65.00	100	0	6.26	16.03
RADAR ENGINEERING	REC 065	N.A.				N.A.				13	13	68.79	100	0	N.A.	N.A.
Overall Pass%		91.43				84				100					100.00	16.00
Class Average		55.09				52.25				65.14					65.14	12.89

Subject Name	Code	Faculty Name
INDUSTRIAL MANAGEMENT	RAS 601	Prof. Sunil Kr Pandey (ME)
CYBER SECURITY	RUC 601	Prof. Sameer Anand (EN)
CONTROL SYSTEM 1	RIC 603	Prof. Myurika Saxena
MICROWAVE ENGINEERING	REC 601	Prof. Praveen Chourasia
DIGITAL COMMUNICATION	REC 602	Prof. Balwant Singh
ADVANCE DIGITAL DESIGN USING VERILOG	REC 064	Prof. Pankaj Goel
RADAR ENGINEERING	REC 065	Prof. Arjun Singh Katiyar



(HOD, ECE) 05/08/2020

S ENGINEERING COLLEGE, GHAZIAB D

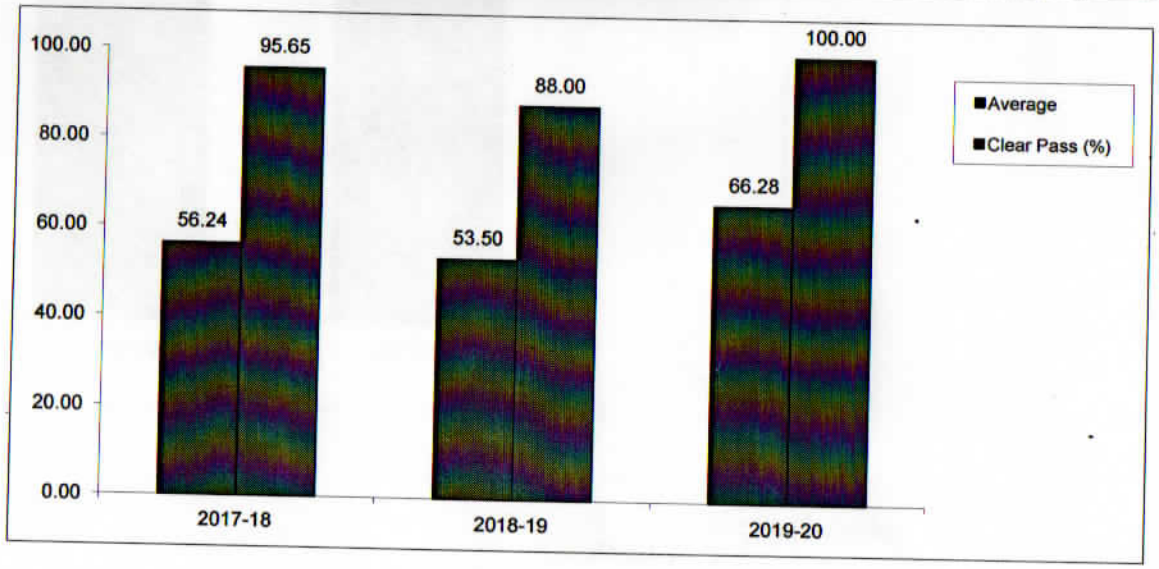
Department of Electronics & Communication Engineering

Result Analysis for EC2 3rd Year Even Semester 2019-20

Subject Name	Subject Code	Session: 2017-18				Session: 2018-19				Session: 2019-20					Avg Diff. wrt 2017-18	Avg Diff. wrt 2018-19
		Students	Average	Pass %	CP	Students	Average	Pass %	CP	Students	Result Declared	Average	Pass %	CP		
INDUSTRIAL MANAGEMENT	RAS 601	46	58.22	100	0	50	57.06	100	0	36	36	66.51	100	0	8.29	9.45
CYBER SECURITY	RUC 601	N.A.				50	58.97	100	0	36	36	66.03	100	0	N.A.	7.06
CONTROL SYSTEM 1	RIC 603	46	56.89	100	0	50	54.57	100	0	36	36	66.27	100	0	9.38	11.70
MICROWAVE ENGINEERING	REC 601	46	56.04	100	0	50	51.37	94	3	36	36	66.11	100	0	10.07	14.74
DIGITAL COMMUNICATION	REC 602	46	54.22	97.82	1	50	50.31	94	3	36	36	66.51	100	0	12.29	16.20
ADVANCE DIGITAL DESIGN USING VERILOG	REC 064	46	60.56	100	0	50	48.74	96	2	23	23	67.08	100	0	6.52	18.34
RADAR ENGINEERING	REC 065	N.A.				N.A.				13	13	64.84	100	0	N.A.	N.A.
Overall Pass%		95.65				88				100.00					4.35	12.00
Class Average		56.24				53.50				66.28					10.04	12.78

Subject Name	Code	Faculty Name
INDUSTRIAL MANAGEMENT	RAS 601	Prof. Sunil Kr Pandey (ME)
CYBER SECURITY	RUC 601	Prof. Sameer Anand (EN)
CONTROL SYSTEM 1	RIC 603	Prof. Praveen Kumar
MICROWAVE ENGINEERING	REC 601	Prof. Praveen Chourasia
DIGITAL COMMUNICATION	REC 602	Prof. Balwant Singh
ADVANCE DIGITAL DESIGN USING VERILOG	REC 064	Prof. Pankaj Goel
RADAR ENGINEERING	REC 065	Prof. Arjun Singh Katiyar

(HOD, ECE) 05/08/2020



DR. A.P.J. ABDUL KALAM TECHNICAL UNIVERSITY UTTAR PRADESH
डॉ0 ए0पी0जे0 अब्दुल कलाम प्राविधिक विश्वविद्यालय उत्तर प्रदेश
(Formerly Uttar Pradesh Technical University)
Sector- 11, Jankipuram Vistar Yojna , Sitapur Road, Lucknow (U.P.) 226031
E-Mail Id: deanugseoffice@aktu.ac.in, dean.ugse@aktu.ac.in

पत्रांक : ए0के0टी0यू0 / डीन यू0जी0 / 2019 /337 दिनाँक: 17 अक्टूबर, 2019

सेवा में,

निदेशक / प्राचार्य
डा0 ए0पी0जे0 अब्दुल कलाम प्राविधिक विश्वविद्यालय उत्तर प्रदेश
से समस्त सम्बद्ध संस्थाएं।

विषयः **Regulations for Challenge Evaluation of Answer Scripts के नये नियमों (सत्र 2018–19) के संबंध में।**

महोदय,

उपर्युक्त विषयक के संबंध में अवगत कराना है कि विश्वविद्यालय की 64वीं परीक्षा समिति की दिनांक 05 फरवरी, 2019 को सम्पन्न बैठक में **Challenge Evaluation** के नियमों में संशोधन किया गया है जो संलग्न कर प्रेषित है। परीक्षा समिति द्वारा लिये गये निर्णय एवं नये नियमों का अनुपालन सम सेमेस्टर सत्र 2018–19 से प्रभावी है।

अतः उपरोक्त संबंध में अनुरोध है कि तद्नुसार छात्रों को अवगत कराने का कष्ट करें। यह सूच्य है कि **Challenge Evaluation** के बाद वास्तविक अंक ही माने जायेगें तथा **Challenge Evaluation** के बाद अंको में बदलने से यदि सत्र परिवर्तित होता है तो छात्रों को परीक्षाफल घोषित दिनांक से उपस्थित मानी जायेगी और छात्र हित में संस्थान द्वारा अतिरिक्त कक्षाएं आयोजित कर पाठ्यक्रम पूर्ण संबधित कार्यवाही करायी जायेगीं।

भवदीय

(प्रो0 सुबोध वैरिया)
डीन0यू0जी0एस0ई0

पृष्ठांकन सं0 एंव दिनांकः उपरोक्त।

प्रतिलिपि– निम्नलिखित को सूचनार्थ एवं आवश्यक कार्यवाही हेतु प्रेषित।

1. कुलसचिव, ए0के0टी0यू0, लखनऊ।
2. परीक्षा नियंत्रक, ए0के0टी0यू0, लखनऊ।
3. स्टाफ आफिसर, मा0 कुलपति कार्यालय, ए0के0टी0यू0, लखनऊ।
4. ई0 आर0 पी0 को इस आशय से प्रेषित उक्त से अच्छादित छात्रो की उपस्थित की व्यवस्था सुनिश्चित कराने का कष्ट करे ।

(प्रो0 सुबोध वैरिया)
डीन0यू0जी0एस0ई0

अ.ग. सं. 64.07 अनुलग्नक-02

REGULATIONS FOR CHALLENGE EVALUATION OF ANSWER SCRIPTS (w.e.f. Odd Sem 2018-19)

1. PREAMBLE

These Regulations shall be called as "**Regulations for Challenge Evaluation of Answer Scripts 2018**" amended from the existing Regulations and approved by the Exam committee.

2. APPLICABILITY:

These Regulations shall come into force from the date of its approved by the Exam committee and these regulations will supersede all the earlier regulations in respect of **Challenge Revaluation**.

3. APPLICATION:

These regulations shall apply to all the undergraduate and postgraduate programs conducted by the University and for persons who have pursued a course of study under all the schemes (changed/changing from time to time) of teaching.

4. DEFINITIONS:

a. "University/AKTU" means Dr. A.P.J. Abdul Kalam Technical University, Lucknow, Uttar Pradesh.
b. "Exam Committee" means, the Examination committee of the University.
c. "COE" means Controller of Examination entrusted with the task of conducting the examinations of University and declaring their results.
d. "College/Institute" means an institution affiliated to or recognized by the University or owned and maintained by it.
e. "Student" means, a person enrolled in the University for taking up studies and/or research.
f. "Teacher/Faculty" means, a person appointed for the teaching purpose posts in the University/Affiliated institutions.

g. "Examiner/revaluator" means teacher/faculty who examine the given answer script and award marks.

h. "Notification" means a letter released by the University inviting applications for Challenge Evaluation mentioning the last dates to apply.

i. "Answer script" means a booklet containing the hand-written answer to questions asked in an examination prepared by a student in the Examination Hall.

j. "Soft copy" means, scanned copy of the answer script.

k. "Challenge Evaluation" means revaluation of answer script to be done by subject examiners who are different from the original examiner who evaluated the answer script in the first instance.

5. CHALLENGE EVALUATION OF ANSWER SCRIPT FOR UNDERGRADUATE AND POST GRADUATE STUDENTS

a. Challenge Evaluation of answer script will be carried out only for the *LATEST* semester whose result has been declared.

b. The students of B.Tech./B.Arch/B.Pharm/BFA/BFAD/BHMCT/MBA/ MCA/M.Tech./M.Arch./M.Pharm/MBA(Int)/MCA(Int) appearing for the University examinations are eligible to apply for Revaluation of answer scripts in all theory subjects.

c. These regulations will also be applicable for Pre-Ph.D courses of research programs.

d. There will be a single notification inviting applications from the students, to apply for Challenge Evaluation of Answer Scripts mentioning the last date.

e. Students may apply for Challenge Evaluation by paying the requisite fee. After the last date, additional time may be granted, subject to the approval from the competent authority. However, under such case, student will have to pay a late fine (non-refundable) for applying for Challenge Evaluation as decided by the university from time to time.

f. A student cannot apply Challenge Evaluation of answer scripts in the subjects other than the *THEORY* subjects.

g. After the last day of application for challenge evaluation, the exam section shall initiate the process of challenge evaluation as per the procedure detailed hereunder:

i. The COE may decide upon the number of evaluation centres in which Challenge Evaluation is to be conducted.

ii. The COE shall direct the directors/coordinators of designated evaluation centre to call the eligible teachers for valuation work (eligibility of teachers to attend Challenge Evaluation is given separately).

iii. Each answer script marked for Challenge Evaluation will be revaluated by two evaluators.

iv. After the revaluation, if the difference between the marks awarded by the two re-evaluators is more than 20% of maximum marks of that subject, then such scripts shall be evaluated once again by a third examiner (who has not evaluated the script in the first valuation).

6. Award of Marks after Revaluation:

i. If the average marks of two revaluators after revaluation is higher/lesser than the original marks, the revaluation marks shall be awarded to the student in that subject.

ii. In case of revaluation as discussed in section **5.g.iv.**, marks to the student shall be awarded in following manner:

CASE: A

If the difference of marks awarded by two revaluators is more than 20% of maximum marks for a given subject, and the answer script is revaluated by a third examiner, average of *Two Nearest Marks* shall be awarded.

First revaluation Marks	*Second revaluation Marks*	*Difference between 1st & 2nd revaluator*	*Third revaluation Marks*	*Final Marks after Revaluation*
15	*40*	*>20%*	*48*	*44*
25	*28*	*≤ 20%*	*Not reqd.*	*27*

CASE: B

When the difference between the nearest two marks in the first, second and the third valuation is approximately equal then the average of *TWO HIGHER MARKS* shall be awarded.

First revaluation Marks	*Second revaluation Marks*	*Difference between 1st & 2nd revaluator*	*Third revaluation Marks*	*Final Marks after Revaluation*
19	*40*	*>20%*	*59*	*50*

v. In case of average being a fraction, for all above cases the awarded mark shall be rounded to the next higher number.

vi. The University will display the Original Marks, Marks after challenge evaluation, on the website and result of the subject will be updated.

7. **Eligibility of teachers for Revaluation:**

The faculty members who will be evaluating the script during revaluation must possess minimum five years of teaching experience and have experience of teaching that subject. If required, expert examiners from other university/institutes not affiliated with AKTU may also be appointed as evaluator.

All previous challenge evaluation rules will cease to exist after implementation of the new regulation.

2015-16

Revised on 21/07/2014

IMS ENGINEERING COLLEGE, GHAZIABAD

APPLICATION FOR SUBMISSION OF FEES FOR CHALLENGE EVALUATION

(ODD/EVEN SEMESTER –)

B.Tech. ☐ MBA ☐ MCA ☐

A. Branch: only for B.Tech. (CE/CS /EC/ IT /EN / ME/BT)_____

B. Name of Student_____ C. Father's Name_____

D. Session_____ E. Semester_____ F. Contact No._____

G. Admission ID._____ H. Roll No._____

I. Subject Name & Code:

S.No.	I/II - Semester		S.No.	III/IV - Semester	
	Subject Code	Subject Name		Subject Code	Subject Name
1			1		
2			2		
3			3		
4			4		
5			5		
6			6		

S.No.	V/VI - Semester		S.No.	VII/VIII - Semester	
	Subject Code	Subject Name		Subject Code	Subject Name
1			1		
2			2		
3			3		
4			4		
5			5		
6			6		

J. Total No. of Subjects: _____ K. Total Amount (in Rs.)_____

(Signature of Student with date)

(For Official Use Only)

Verified by:

(Signature of office staff with date)
Name:

Note: 1. Challenge Evaluation University Exam Fee is @ Rs. 5000/- per subject (It may changed as per university direction).
2. Enclosed copy of result.