Supporting Document

7.2.1 Describe two best practices successfully implemented by the Institution as per NAAC format provided in the Manual.

IMS ENGINEERING COLLEGE, GHAZIABAD

Counselor Card

Student Information :

Name: Anamika Singh **Roll No.** 1614321012 **Dept/Section** EN 1

Permanent Address : Vill-Post: Heeranpatti, Azamgarh (U.P.)

Present Address : IMS Girls Hostel No. 101
IMS Girls Hostel Room no. 430

Family Background : father: Mr. Dharmendra Singh (Business) 9454000811
Mother: Mrs. Kiran Singh (Housewife) 9451751278
Brother: Anshuman Singh

Student's Interest/ Aspiration : Study, want to qualify GATE

Academic Performance :

Pre-Admission : 10th ICSE: 80%, 12th: ISC: 78%, PCM:

1st Semester	811, CP = 0	2nd Semester	831, CP = 0
3rd Semester	902, CP=0	4th Semester	854/1000, CP=0
5th Semester	930/1000, CP=0	6th Semester	849/1000, CP=0
7th Semester	897/1000, CP=0	8th Semester	904/1000, CP=0

Extra-Curricular Achievements :

→ Participated in "TECHNOVATION-2017" & won the consolation prize
→ Branch topper in I-Year.
→ Participated in "Technovation-2018" & won the 3rd prize.

Disciplinary Action Taken :

Counseling Details

1st Semester			Counselor : Sujeet Kumar Srivastava				
Sessional Test-1 Marks/Attendance	REE101 30/100	RAS101 26/100	RAS103 29/100	RAS104 22/100	REC101 25/100		
Sessional Test-2 Marks/Attendance	19/100	18/100	20/100	14/94	21/96		
Pre-Semester	98	88	97	82	90		

Date / Time	Brief counseling Agenda	Future Action/Action Taken
23/08/16	No Problem.	Work hard
3/10/16	Very Good performance.	Advice to be focus in english subjects

2nd Semester			Counselor : Sujeet Kumar Srivastava				
Sessional Test-1 Marks/Attendance	RAS201 28	RAS202 29	RAS203 28	RAS201 23	RME201 30		
Sessional Test-2 Marks/Attendance	23	30	30	30	28		
Pre-Semester	63	60	69	68	67		

Date / Time	Brief counseling Agenda	Future Action/Action Taken
8/2/17	No problem, performance is very good.	
10/04/17	very good	

Counseling Details

3rd Semester			Counselor : Gyanesh Singh				
Sessional Test-1 Marks/Attendance	RAS-301 29	RVE-302 22	REC-309 28	REE 301 26	REE 302 29	REE 303 30	93% (Attendance)
Sessional Test-2 Marks/Attendance	30	26	29	27	A	25	
Pre-Semester	69	54	67	68	69	70	

Date / Time	Brief counseling Agenda	Future Action/Action Taken
14/Sep/17	Regarding 1st sessional Examation	Excellent Keep it up
14/10/17	Improvement	Good keep it up.

4th Semester			Counselor : Varun Kr Singhal				
Sessional Test-1 (30) Marks/Attendance	REE-047 29	RAS-402 28	REC-402 28	REE-401 21	REE-402 29	REE-405 26	% Att. 98
Sessional Test-2 (30) Marks/Attendance	A	A	29	29	28	25	
Pre-Semester (70)	65	57	66	63	67	69	96

Date / Time	Brief counseling Agenda	Future Action/Action Taken
22/2/18 (11:30 AM)	→ Regarding 3rd Sem. result	→ Appreciated her
29/3/18 (4:00-4:05 AM)	→ Performance of CT-1	→ Appreciated her & motivated her to appear in CT-2

Counseling Details

5th Semester / 6th Semester — **Counselor:** Varun Kr Singhal

	REE 501	REE 502	REE 503	REE 052	RAS 501	RAS 502	RAS 601	RAS 601	REE 601	REE 602	REE 603	REE 064	Att.
Sessional Test-1 Marks/Attendance	29	29	29	26			29	25	30	29	28	29	97%
Sessional Test-2 Marks/Attendance	30	24	27	28	27 A	22 A	A	A	30	29	29	A	
Pre-Semester	67	70	69	67	64	62	66	46	67	66	63	67	94%

Date / Time	Brief counseling Agenda	Future Action/Action Taken
30/8/18	→ Regarding Previous sem. Result → TechFest	→ Motivated her to participate in TechFest.
1/10/18	→ Performance of CT-1	→ Motivated her to appear in CT-2
25/2/19	→ university result of 5th sem.	→ Appreciated her for getting highest marks in 3rd year.
19/4/19	→ PUT & Final Exam.	→ Motivated her

7th Semester / 8th Semester — **Counselor:** Varun Kumar Singhal

	REG 071	REN 701	REN 075	REE 702	ROE-071	ROE-082	REN-080	REE-085	
Sessional Test-1 Marks/Attendance	26	29	29	30	21	A	25	A	
Sessional Test-2 Marks/Attendance	A	A	A	A	A	24	30	30	
Pre-Semester	66	60	62	68	54				

Date / Time	Brief counseling Agenda	Future Action/Action Taken
14/8/19	→ 6th sem. University result → Gold Medal in Final Year	→ Motivated her for Goldmed in Final year as she was the topper of EN 3rd year.
15/10/19	→ Academic Award → Placement	→ Motivated and appreciate her.
19/2/20	→ 7th sem. Result, Placement	→ Appreciated her and motiv for Gold Medal. → Encouraged her to appear all placement drives.

IMS Engineering College, Ghaziabad

Minutes of Meeting

A meeting of Deans & HODs was held by Director in the Conference Room on 8th August, 2015 (Saturday) at 10:00 AM. Following members were present in the meeting:

1. Dr. Sraban Mukherjee, Director
2. Mr. Sanjay Kumar, Dean (Academic)
3. Mr. Pankaj Goel, Dean (SW)
4. Dr. S.N. Rajan, Dean (R&D)
5. Dr. Neetu Goel, Dean (AS&H)
6. Dr. Abhimanyu Kr. Jha, HOD (BT)
7. Dr. Monica Verma, HOD (MBA)
8. Dr. Pankaj Agarwal, HOD (CS)
9. Mr. N.U. Khan, HOD (IT)
10. Dr. V.K. Saini, HOD (ME/CE)
11. Dr. R.P.S. Chauhan, HOD (EC)
12. Dr. Rishi Asthana, HOD (EN)

Agenda of the Meeting:

Following was the agenda of the meeting:

1. To review of Academic Progress
2. Class attendance/strength of students in classes
3. Any other item

Minutes of Meeting:

Director welcomed all the members and following points were discussed/ decided:

1. GP Marks allocation scheme should be notified. Students should be notified about the status of their attendance before sessional examinations. GP Marks are to be given as per practice. Any change in GP Marks should be notified before the session/semester starts.
2. Time-table of the MBA department faculty member (taking classes in B.Tech) needs to be modified since they have been shifted to IMS-UC Campus.

3. Quantitative aptitude classes to be conducted for BT students also for TCS test.
4. Number of assignments in theory (which are 10 at present) to be reduced.
5. In Mathematics assignments, there should be tutorials only. In CCP, Unit-I may be taught later and Unit-II to start first.
6. Assignments marks to be decided at the time of finalization of sessional marks.
7. The Director emphasized to improve placement of students.
8. Final year students' placement activities are to be coordinated by class coordinators. Attendance benefit to students is to be given on recommendation of class coordinators.
9. Students counseling should be made more effective for their growth and improvement. There will be 2 counsellors in every class/section and half of the students will be allotted to each of them. They will interact with students, identify their problems, if any, and will further counsel them.
10. AS&H departments to be shifted in Academic Block-A with immediate effect.
11. HODs to submit corrected faculty load.
12. Proctorial Board members need to watch students in front of Block-B&C as per earlier practice as the new session has commenced.
13. Under PDP Programme, the faculty not to teach communication only rather on GD & PI practice.
14. Aptitude classes not only to focus on TCS but should also focus on other examinations like CAT etc.
15. For Aptitude Tests, crash course to be done for which negotiation is already going on. Classes to start from 17th August, 2015 probably. 60 plus students (between 50-75 students) may be accommodated in a class.
16. MAT Lab software to be re-installed in Lab systems (EN).
17. Class attendance to be sent to Director on daily basis by 11:30 AM.

18. Technical exhibitions are to be organized. Only 2nd, 3rd and 4th year students (excluding MBA students) are to do projects for technical exhibitions. HODs to ensure that maximum number of students participate in it. **19th & 20th October, 2015** have been decided as dates for Technical exhibitions. Attendance to be given to students for project works for Technical exhibitions on recommendation of Technical Exhibition Co-ordinators. Prof. S.N. Rajan and two faculty from 1st year will be responsible for organization Technical Exhibitions.

19. HODs to send requirement of LCD projector in different departments, if any. All computer labs should have LCD projectors.

20. A Centre of Excellence for Robotics should be established. Two faculty each from ME & CS may be identified for Robotics Lab. **[Action HOD (ME) & HOD (CS)]**

ATTENDANCE REGISTER CHECKING (CE) Inbox ×

Ankur Gupta <ankur.gupta@imsec.ac.in> Nov 22, 2016, 10:55 AM

to Suman, me, Saurabh, Ketan, Pradeep, Vivek, Amit, Uday

All the faculty members are requested to complete all the entries in attendance register & counselling cards (to whomsoever have been allotted) and show it to Prof J.P Mani latest by 23/11/2016. Also get the attendance register signed by the HOD, Dr. V.K. Saini.

Regards.

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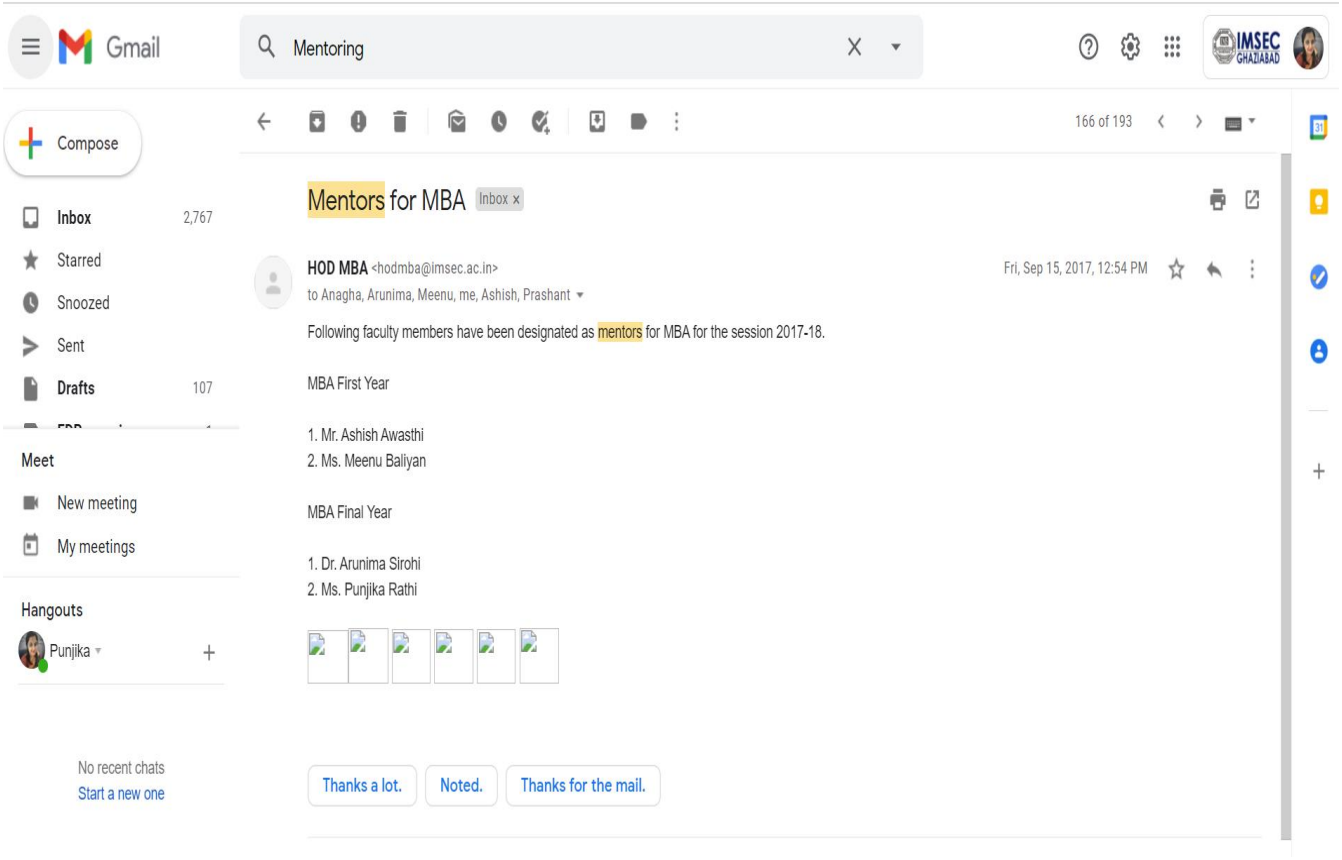
Ankur Gupta
Asst. Professor
Civil Engineering Department
IMS Engineering College, Ghaziabad


Gmail
Mentoring
IMSEC GHAZIABAD
Compose
Inbox 2,767
Starred
Snoozed
Sent
Drafts 107
Meet
New meeting
My meetings
Hangouts
Punjika
No recent chats
Start a new one
166 of 193
Mentors for MBA
Inbox ×
HOD MBA <hodmba@imsec.ac.in>
to Anagha, Arunima, Meenu, me, Ashish, Prashant
Fri, Sep 15, 2017, 12:54 PM
Following faculty members have been designated as mentors for MBA for the session 2017-18.
MBA First Year
1. Mr. Ashish Awasthi
2. Ms. Meenu Baliyan
MBA Final Year
1. Dr. Arunima Sirohi
2. Ms. Punjika Rathi
Thanks a lot.
Noted.
Thanks for the mail.

COURSE FILE

OF

Integrated Circuits

(KEC 501)

2020-2021

DEPARTMENT OF

ELECTRONICS & COMMUNICATION

ENGINEERING

IMS ENGINEERING COLLEGE, GHAZIABAD

Faculty Name: Praveen Kumar

Branch: Electronics and Communication *Engineering*

Semester: 5th

Session: 2020-21

Subject Name: Integrated Circuits

Subject Code: KEC 501

IMS ENGINEERING COLLEGE	IMSEC/QF/42
FORMATS	Page 1 of 1 Issue No: 02
Course File Cover Page	Issue Date: 1 May 2010
Prepared by: MR	Approved by: Director

	Particulars
1.	Quality Policy (on left inside cover of Course File)
2.	Institute Mission and Vision
3.	Departmental Mission and Vision
5.	Program Outcomes (PO)
6.	Program Educational Objectives (PEO) and Program Specific Outcomes (PSO)
7.	Academic Calendar
8	Time Table
9	Student List
10.	University Evaluation Scheme
11.	Syllabus (Theory)
12.	Course Outcome, Mapping with PO/PSO
13.	Syllabus (Practical) with Experiment List mapped with Course Outcomes
14.	Topics beyond Syllabus
15.	Quiz/Assignment/Tutorial Records
16.	CT Question Paper (mapped with CO)
17.	Sessional Marks Analysis
18.	Lecture Notes/PPT
19.	Question Bank
20	Last three years University Question Paper (AKTU) with Solution
21	Attendance Register

Name and Signature of Course Instructor	Signature of HoD
Praveen Kr	

Space for Internal Auditor's Use

IMSEC, GHAZIABAD

Department of Electronics and Communication Engineering

Vision of the Institution

Our vision is to impart vibrant, innovative and global education to make IMS the world leader in terms of excellence of education, research and to serve the nation in the 21st century.

Mission of the Institution:

- To develop IMSEC as a centre of Excellence in Technical and Management education.
- To inculcate in its students the qualities of Leadership, Professionalism, Executive competence and corporate understanding.
- To imbibe and enhance Human Values, Ethics and Morals in our students.
- To transform students into Globally Competitive professionals.

Vision (Department):

To produce highly competent engineers by imparting innovative and accomplished information through global education and adequately prepare them to face the challenges of outside world by fulfilling the requirements of Electronics & Communication industries.

Mission (Department):

- To make the department a centre of excellence in Electronics & Communication Engineering and to produce eminent engineers.
- To inculcate professionalism, team work, leadership qualities by imbibing high human values and professional ethics, in students.
- To enhance the employability of students by giving inter-disciplinary knowledge to meet the need of society and become globally competitive professionals.
- To become a centre for research in the stream of Electronics & Communication Engineering and to provide excellent learning environment for researchers by promoting research activities in the department.

IMSEC, GHAZIABAD

Department of Electronics and Communication Engineering

PROGRAM OUTCOMES (POs)

1. **Engineering knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization for the solution of complex engineering problems.
2. **Problems analysis:** Identify, formulate, research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design development and solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for public health and safety and cultural, societal and environmental considerations.
4. **Conduct investigations of complex problems:** Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.
5. **Modern tool usage:** Create, select, and apply appropriate techniques, resources and modern engineering IT tools, including prediction and limitations.
6. **The engineer and society:** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts and demonstrate the knowledge of and need for sustainable development.
8. **Ethics:** Apply ethical principles, commit to professional ethics, responsibilities and norms of the engineering practice.
9. **Individual and team work:** Function effectively as an individual, as a member or leader in diverse teams and in multidisciplinary settings.
10. **Communication:** Communicate effectively on complex engineering activities with the engineering community and with the society at large. To be able to comprehend and write effective reports, design documentation, make presentations, give and receive clear instructions.
11. **Project management and finance:** Demonstrate knowledge, understanding of the engineering and management principles. Apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.
12. **Life-long learning:** Recognize the need for and have the preparation, ability to engage in independent and life-long learning in the broadest context of technological change.

IMSEC, GHAZIABAD

Department of Electronics and Communication Engineering

Program Educational Objectives (PEOs)

PEO1: Graduates will excel in Electronics & Communication Engineering, both in industrial and academic sector by applying their technical skills and knowledge in a professional manner.

PEO2: Graduates will be capable of effectively analyzing and solving engineering problems utilizing appropriate techniques and advanced engineering tools.

PEO3: Graduates will be capable of applying their knowledge both in individual and multidisciplinary environments. They will also demonstrate excellent communication skills and caliber to work as a team.

PEO4: Graduates will realize the significance of environmental concerns while keeping safety, ethical and societal values into consideration.

PEO5: Graduates will be capable of implementing outputs derived from research based knowledge in projects, analysis and interpretation of data leading to development of new processes and systems.

IMSEC, GHAZIABAD

Department of Electronics and Communication Engineering

PROGRAM SPECIFIC OUTCOMES (PSOs)

At the end of the program, the students will have:

1. An ability to exhibit knowledge acquired from mathematics, engineering fundamentals, Electronics & Communication engineering and related fields for professional excellence in industry and research organizations.
2. An ability to solve and communicate complex Electronics and Communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive at cost effective and appropriate solutions.
3. Wisdom of social and environmental awareness along with ethical responsibility to have a successful career and to sustain passion and zeal for real-world applications using optimal resources as an Entrepreneur.
4. An ability to select appropriate techniques , resources for execution of projects and function effectively as an individual as well as a team member in multidisciplinary diverse environments.

IMS ENGINEERING COLLEGE, GHAZIABAD
ACADEMIC CALENDAR (As per AKTU) (ODD SEM: 2020 - 21) [Version-1]

Oct-20

M	T	W	T	F	S	S
			1	2	3	4
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28	29	30	31	

T/ W Days : 19/21

Nov-20

M	T	W	T	F	S	S
						1
2	3	4	5	6	7	8
9	10	11	12	13	14	15
16	17	18	19	20	21	22
23	24	25	26	27	28	29
30						

T/ W Days : (16+3)/20

Dec-20

M	T	W	T	F	S	
	1	2	3	4	5	6
7	8	9	10	11	12	13
14	15	16	17	18	19	20
21	22	23	24	25	26	27
28	29	30	31			

T/ W Days : 17/24

Jan-21

M	T	W	T	F	S	S
				1	2	3
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29	30	31

T/ W Days : 15/22

Feb-21

M	T	W	T	F	S	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28

T/ W Days : 20/22

Mar-21

M	T	W	T	F	S	
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				

T/ W Days : 5/23

IMPORTANT DATES	HOLIDAYS	EXAMINATION / CLASS TEST
Commencement of Classes for 2nd, 3rd & 4th Yr: 5th Aug	**14, 15 & 16 NOV (SAT, SUN & MON):** Deepawali	CT-1 : 2nd-DEC to 8thDEC, 2020
Commencement of Classes for 1st & 2nd (Lateral) 25th NOV	**30-NOV (MON) :** Guru Nanak's B'day	CT-2 : 19, 21, 26, 28-DEC, 2, 4 JAN 2021
	25-DEC (FRI) : Christmas Day	PUT : 18th JAN to 23rd JAN, 2021
	11-MAR (THU) : Maha Shivratri	(3rd & 4th Year AKTU External)
Upload Assignment (Important Dates)	**28-MAR (SUN) :** Holika Dahen	AKTU End Sem Exam (01-FEB to 20-FEB, 2021)
	29-MAR (MON) : Holi	(1st & 2nd Year AKTU External)
		AKTU End Sem Exam (08-MAR to 20-MAR, 2021)
		AKTU End Sem Practical Examination

Total Teaching Days/Working Days (T/W) : 60/132 [95/132]

Faculty members are requested to 1) Upload the attendance after completion of the class (L/T/P) itself on the same day.
2) Upload / Check / Submit the assignment as per schedule (weekly).

IMS ENGINEERING COLLEGE	IMSEC/QF/08b
FORMAT	Page 1 of 1
	Issue No: 01
Time Table	Issue Date: 1 May 2010
Prepared by:	Approved by: Director

CLASS TT EC-2 4th YEAR (C-306)

Academic Session2020-21(ODD)

DAY/TIME	Period-1	Period-2	Period-3	Period-4	Break	Period-5	Period-6
	9:00-9:50	10:00-10:50	11:00-11:50	12:00-12:50	12:50-2:00 PM	2:00-2:50 PM	3:00-3:50 PM
MON			KEC 301			Electronics Devices Lab	
TUE	KEC 301	KEC 301				Integrated Circuits Lab	
WED			KEC-501				
THU		KEC 301				KEC-501	
FRI	KEC-501			KEC-501			
SAT							

CODE	Subject	FACULTY	Code	Lab Name	
KEC-501	Integrated Circuits	PROF PRAVEEN KUMAR	KEC 351	Electronics Devices Lab	
KEC-701	Electronic Devices	PROF PRAVEEN KUMAR	KEC 551	Integrated Circuits Lab	

IMS ENGINEERING COLLEGE GHAZIABAD

ELECTRONICS & COMMUNICATION ENGINEERING DEPARTMENT

EC 3rd year

S.No.	Roll No.	Name	Student No.	Father No.
1	1714331042	RAHUL SINGH	8512846443	
2	1814331002	AASHI SINGH	9760844799	7253090799
3	1814331004	ABHISHEK KANDPAL	8929297923	9810334103
4	1814331003	ABHISHEK KUMAR	7352133304	9348555526
5	1814331005	ADITYA KUMAR	7524056794	9598271523
6	1814331006	ADITYA PANDEY	9628647442	9005808762
7	1814331007	AKHIL RUHELA	7838954908	9953004133
8	1814331008	AKSHAY VERMA	7017889514	9410267058
9	1814331009	ALI MAJAZ	8191919749	9634371978
10	1814331010	AMAN SAIFI	9897940786	9897940786
11	1814331011	ANIRUDH MANOJ	8006060404	8006060404
12	1814331012	ANMOL SHARMA	8588861488	9871589567
13	1814331013	ANSHUL SHARMA	9899062918	7428572447
14	1814331014	ANTRIKSH SAXENA	8057290569	9639971946
15	1814331015	ANUBHAV SINGH	9536712418	6396061138
16	1814331016	ARBAZ AKHTAR	7905325543	9540080461
17	1814331028	ARMAN SHAH	9910636028	9958139757
18	1814331017	ARPIT SONI	7607524723	8423002715
19	1814331018	ASHISH CHAUDHARY	7453039250	9719057509
20	1814331019	ASHISH SHARMA	9105212161	9927365600
21	1814331020	AYUSH SAINI	7060050264	9368007688
22	1814331021	HARDIK RASTOGI	8265983373	9837048602
23	1814331022	HARSH JAISWAL	7651966994	9450630124
24	1814331023	JATIN AGARWAL	8171008360	9897046135
25	1814331024	JATIN RANA	9311663355	9871023868
26	1814331025	JAYA SINHA	9354773714	8966841558
27	1814331026	KRITIKA NATH	7530845511	9971381759
28	1814331032	MANIK CHOUDHARY	8082640017	9055072582
29	1814331027	MANSI SAXENA	9794790063	9044879071
30	1814331029	MUDIT PRATAP SINGH	9415998182	9451466553

31	1814331030	MUKUL CHAUHAN	8859977600	8859977600
32	1814331031	MUNESH KUMAR SINGH	7007912346	9952709172
33	1814331033	NIKHIL KUMAR	8192828586	9410653845
34	1814331034	NISHA .	9821151993	9716598366
35	1814331035	NITESH UPADHYAY	8006041323	8006041323
36	1814331036	PRABHAT MITTAL	9457625151	9410224751
37	1814331037	PRADEEP DUBEY	9598900234	7532989975
38	1814331038	PRAKHAR TRIVEDI	9554604065	9415474508
39	1814331039	RACHIT GARG	9717182905	9667223326
40	1814331040	RISHABH GUPTA	7081168512	9026374265
41	1814331041	RIYA AGARWAL	9412659808	9837654012
42	1814331042	SAKSHI VARSHNEY	7455007178	9058464594
43	1814331043	SARANSH RAI	9682290100	9532706590
44	1814331044	SARTHAK GUPTA	9784546866	9887859633
45	1814331045	SAURABH GUPTA	8382814157	9984160785
46	1814331046	SHASHWAT DWIVEDI	9161133639	9090973080
47	1814331047	SHELENDRA RAGHAV	9868937012	8130603668
48	1814331048	SHIVAM KATIYAR	9354483513	9654958542
49	1814331049	SHIVANGI MISHRA	9532215002	8800108462
50	1814331050	SUPREET DEOL	8160586479	9927647574
51	1814331051	TANISH VARSHNEY	7906229438	9219758815
52	1814331052	TANISHKA VATS	8810335918	9599612689
53	1814331053	TUSHAR KUMAR	7906365288	7060153909
54	1814331054	UTKARSH SINGH	6351611541	7228888653
55	1814331055	VED PRAKASH SHARMA	9472207260	9631623631
56	1814331056	VISHAL RANA	7839801507	8650664356
57	1814331057	YASH DIXIT	8279724868	9917022660
58	1814331058	YASHASVI SINGH	9956441270	9918164501

B.Tech. V Semester
Electronics and Communication Engineering

S. No.	Course Code	Course Title	Periods			Evaluation Scheme				End Semester		Total	Credits
			L	T	P	CT	TA	Total	PS	TE	PE		
1	KEC-501	Integrated Circuits	3	1	0	30	20	50		100		150	4
2	KEC-502	Microprocessor & Microcontroller	3	1	0	30	20	50		100		150	4
3	KEC-503	Digital Signal Processing	3	1	0	30	20	50		100		150	4
4	KEC-051–054	Department Elective-I	3	0	0	30	20	50		100		150	3
5	KEC-055-058	Department Elective-II	3	0	0	30	20	50		100		150	3
6	KEC-551	Integrated Circuits Lab	0	0	2				25		25	50	1
7	KEC-552	Microprocessor & Microcontroller Lab	0	0	2				25		25	50	1
8	KEC-553	Digital Signal Processing Lab	0	0	2				25		25	50	1
9	KEC-554	Mini Project/Internship **	0	0	2				50			50	1
10	KNC501/KNC502	Constitution of India, Law and Engineering / Indian Tradition, Culture and Society	2	0	0	15	10	25		50			NC
11		MOOCs (Essential for Hons. Degree)											
		Total										**950**	**22**

**The Mini Project or Internship (4weeks) conducted during summer break after IV Semester and will be assessed during Vth Semester.

Course Code	Course Title
	Department Elective-I
KEC-051	Computer Architecture and Organization
KEC-052	Industrial Electronics
KEC-053	VLSI Technology
KEC-054	Advance Digital Design using Verilog
	Department Elective-II
KEC-055	Electronics Switching
KEC-056	Advance Semiconductor Device
KEC-057	Electronics Measurement & Instrumentation
KEC-058	Optical Communication

KEC-501	INTEGRATED CIRCUITS	3L:1T:0P	4 Credits

Unit	Topics	Lectures
I	**The 741 IC Op-Amp**: General operational amplifier stages (bias circuit, the input stage, the second stage, the output stage, short circuit protection circuitry), device parameters, DC and AC analysis of input stage, second stage and output stage, gain, frequency response of 741, a simplified model, slew rate, relationship between ft and slew rate.	8
II	**Linear Applications of IC Op-Amps:** Op-Amp based V-I and I-V converters, instrumentation amplifier, generalized impedance converter, simulation of inductors. **Active Analog filters:** Sallen Key second order filter, Designing of second order low pass and high pass Butterworth filter, Introduction to band pass and band stop filter, all pass active filters, KHN Filters. Introduction to design of higher order filters.	8
III	**Frequency Compensation & Nonlinearity:** Frequency Compensation, Compensation of two stage Op-Amps, Slewing in two stage Op-Amp. Nonlinearity of Differential Circuits, Effect of Negative feedback on Nonlinearity. **Non-Linear Applications of IC Op-Amps:** Basic Log–Anti Log amplifiers using diode and BJT, temperature compensated Log-Anti Log amplifiers using diode, peak detectors, sample and hold circuits. Op-amp as a comparator and zero crossing detector, astable multivibrator & monostable multivibrator. Generation of triangular waveforms, analog multipliers and their applications.	4 8
IV	**Digital Integrated Circuit Design:** An overview, CMOS logic gate circuits basic structure, CMOS realization of inverters, AND, OR, NAND and NOR gates. **Latches and Flip flops**: the latch, CMOS implementation of SR flip-flops, a simpler CMOS implementation of the clocked SR flip-flop, CMOS implementation of J-K flip-flops, D flip- flop circuits.	6
V	**Integrated Circuit Timer:** Timer IC 555 pin and functional block diagram, Monostable and Astable multivibrator using the 555 IC. Voltage Controlled Oscillator: VCO IC 566 pin and functional block diagram and applications. **Phase Locked Loop (PLL)**: Basic principle of PLL, block diagram, working, Ex-OR gates and multipliers as phase detectors, applications of PLL.	6

Text Book:

1. Microelectronic Circuits, Sedra and Smith, 7th Edition, Oxford, 2017.
2. Behzad Razavi: Design of Analog CMOS Integrated Circuits, TMH

Reference Books:

1. Gayakwad: Op-Amps and Linear Integrated Circuits, 4th Edition Prentice Hall of India, 2002.
2. Franco, Analog Circuit Design: Discrete & Integrated, TMH, 1st Edition.
3. Salivahnan, Electronics Devices and Circuits, TMH, 3rd Edition, 2015
4. Millman and Halkias: Integrated Electronics, TMH, 2nd Edition, 2010

Course Outcomes: At the end of this course students will demonstrate the ability to:

1. Explain complete internal analysis of Op-Amp 741-IC.
2. Examine and design Op-Amp based circuits and basic components of ICs such as various types of filter.
3. Implement the concept of Op-Amp to design Op-Amp based non-linear applications and wave-shaping circuits.
4. Analyse and design basic digital IC circuits using CMOS technology.
5. Describe the functioning of application specific ICs such as 555 timer ,VCO IC 566 and PLL.

IMS ENGINEERING COLLEGE,GZB		
Sessional Question Paper	IMSEC/QF/49	
	Page 1 of 1	
	Issue no: 02	
	Issue date: 1 May 2010	
1st Sessional Examination (CT-1), Odd Sem. 2019-20		
Subject Name: Integrated Circuits	Subject code	REC 501
Roll No. of student	Max Marks	30
	Max time	1:30hrs
For EC1, EC2 3rd Year	Approved By Director	

Note: Attempt any *six* questions (6×5=30)

Q.1 What are the desirable characteristics of current mirror circuit? Draw the simple BJT current mirror circuit and derive the expression of current transfer ratio.

Q.2 For V_{dd} = 1.8V and using I_{REF} = 50μA. It is required to design the circuit of Fig.1 to obtain an output current whose nominal value is 50μA. Find R if Q_1 and Q_2 are matched with channel lengths of 0.5μm, channel widths of 5μm, V_t = 0.5V and k_n' = 250μA/V². What is the lowest possible value of V_o? Assuming that for this process technology the early voltage V'_A = 20V/μm, find the output resistance of current source.

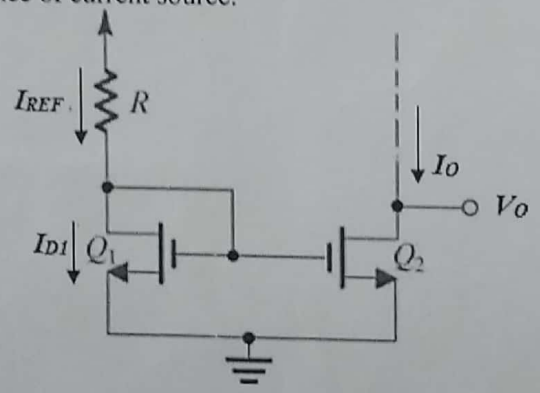


Fig.1

Q.3 Explain Wilson Current mirror. How the V_{DS} mismatching is avoided by improved Wilson mirror?

Q.4 Draw the circuit diagram of cascode current mirror; also write the advantage and disadvantage of cascode current mirror.

Q.5 Design a CMOS full adder circuit with inputs A, B, C and two output S and C_0.

Q.6 Sketch the CMOS realization of the following Boolean function-

(a) $Y = \overline{(A+B+C).D}$ (b) $Y = \bar{A}B + A\bar{B}$

Q.7 Sketch the CMOS implementation of SR flip-flop and explain its working.

Q.8 Draw the D-flip flop using CMOS. Also draw and explain its master slave configuration.

For office use only					
Course Outcomes and Question mapping matrix					
CO1	CO2	CO3	CO4	CO5	CO6
Q. 1, 2, 3, 4	-	Q. 5, 6, 7, 8	-	-	-

Chauhan 30/08/19

IMSENGINEERINGCOLLEGE,GZB		
Sessional Question Paper	IMSEC/QF/49	
	Page 1 of 1	
	Issue no: 02	
	Issue date:1 May 2010	
2nd Sessional Examination (CT-2), Odd Sem. 2019-20		
Subject Name: Integrated Circuits	Subject code	REC 501
Roll No. of student	Max Marks	30
	Max time	1:30hrs
For EC1, EC2 3rd Year	Approved By Director	

Note: Attempt any ***six*** questions (6×5=30)

Q.1 Draw the generalized impedance converter and derive its impedance equation. Also simulate an Inductor.

Q.2 Explain how a Schmitt Trigger circuit works with a neat diagram. Design a Schmitt trigger with V_{UT} = 2V, V_{LT} = -2V. Assume ± V_{sat} = ±13V.

Q.3 Draw the circuit of Sallen Key filter and derive the expression of its transfer function. Also design the equal component Sallen key high pass filter.

Q.4 Derive the expression of voltage gain in KHN biquad filter. Draw the KHN biquad filter and drive transfer function of the BPF and LPF from that.

Q.5 Draw and explain basic logarithmic amplifier. Also explain temperature compensated logarithmic amplifier.

Q.6 Explain the working of precision full wave rectifier with necessary waveform.

Q.7 Design a wide band pass filter with f_l = 500Hz, f_h = 1500Hz and a pass band gain of 4. Draw frequency response of band pass filter and find value of Q.

Q.8 Design a 2nd order low pass Butterworth filter with cut off frequency of 1 KHz.

For office use only					
Course Outcomes and Question mapping matrix					
CO1	CO2	CO3	CO4	CO5	CO6
-	Q. 3, 4, 7, 8	-	Q.2, 5, 6	-	Q.1

07/11/19

IMSENGINEERINGCOLLEGE,GZB		
Sessional Question Paper	IMSEC/QF/49	
	Page 1 of 1	
	Issue no: 02	
	Issue date:1 May 2010	
PUT Examination, Odd Sem. 2019-20		
Subject Name: Integrated Circuits	Subject code	REC 501
Roll No. of student	Max Marks	70
	Max time	3 Hrs
Prepared By: MR	Approved By Director	

Note: All sections are compulsory. If require any missing data; then choose suitably.

Section-A

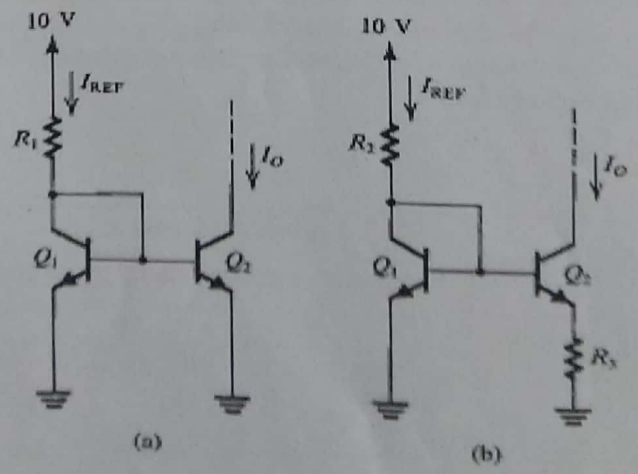
Q.1 Attempt any **seven** parts of this question (2×7=14)

a) What is the advantage of Widlar current source over simple constant current source?
b) Define and give significance of Slew Rate.
c) Write the advantage of active filter over passive filter?
d) What do you mean by a frequency response of a filter circuit?
e) Why CMOS NAND is preferred over CMOS NOR?
f) Give two application of analog multiplier.
g) What is a Super Diode?
h) List the application of PLL.
i) The basic step of a 8-bit DAC is 20mV. If 00000000 represents 0V, what is represented by the input 10110111.
j) What are the advantages of CMOS logic family?

Section-B

Attempt any ***three*** questions of this section. (7×3=21)

Q.2 Explain Widlar current source.
Following Fig. (a) and (b) shows the two circuit for generating a constant current of 10μA which operates from 10V supply. Determine the value of required resistors assuming that V_{BE} = 0.7V at a current of 1mA and neglecting the effect of finite β.



22/11/19

Q.3 Draw the CMOS realization of the following Boolean expression
(i) $Y = \overline{A + B(C + D)}$ (ii) $Y = \overline{(A + B).C + D}$

Q.4 Explain the circuit of following current mirror and also discuss their advantage-
(i) Wilson current mirror (ii) Base current compensated current mirror

Q.5 Explain the following circuit using op-amp
(i) Schmitt trigger (ii) Comparator and zero crossing detector

Q.6 (i) Design a wide band pass filter with f_L = 200Hz, f_H =1KHz and a pass band gain of 4.
(ii) Design a 2nd order Butterworth high pass filter with cut-off frequency of 1KHz.

Q.7 Explain R-2R ladder type digital to analog converter.

Section-C

Attempt ***any one part*** of each questions of this section. (7×5=35)

Q.8 a) Discuss the frequency response of 741opamp. Relate unity-gain bandwidth and slew rate.
b) How the short circuit protection is achieved in the output stage of 741 op-amp?
c) Explain MOSFET current mirror, also show the effect of V_o on I_o.

Q.9 a) Draw the circuit of KHN biquad filter and derive the expression of its voltage gain
b) Realize generalized impedance converter (GIC) with op-amp. How the inductor is simulated using this GIC.
c) Implementation the following filter using op-amp
(i) Notch filter (ii) Narrow band pass filter

Q.10 a) Design a CMOS full adder circuit with three inputs A, B, C and two output S and C_o.
b) Give the CMOS implementation of clocked SR flip-flop and explain its working.
c) Draw the D-flip flop using CMOS. Also draw and explain its master slave configuration.

Q.11 a) Draw and explain the circuit of temperature compensated logarithmic amplifier.
b) Explain working of precision full wave rectifier with necessary waveform.
c) Draw and explain the circuit of square wave generator (astable multivibrator) using op-amp and derive the expression of output frequency.

Q.12 a) Explain the operation of dual slope ADC.
b) Draw and explain the circuit of astable multivibrator using 555 timer. Also derive the expression of frequency and duty cycle of output wave form.
c) Draw the block diagram of a PLL and explain its operation. Explain lock-in-range, capture range and pull-in time of a PLL.

For office use only					
Course Outcomes and Question mapping matrix					
CO1	CO2	CO3	CO4	CO5	CO6
Q.1(a,b), Q.2, Q.4, Q.8	Q.1(c,d), Q.6, Q.9	Q.1(e,j), Q.3, Q.10	Q.1(f, g), Q.5, Q.11	Q.1(i), Q.7, Q.12 (a,c)	Q.1(h), Q.12(b)

IMS Engineering College, Ghaziabad
Department of Electronics & Communication Engineering
PUT Result Analysis (Odd Semester 2019-20)

Class: EC1 3rd Year | Sub: Integrated Circuits (REC 501)

S. No.	University Roll	Name	CT-1 Marks (30)	CT-1 Marks (30)	PUT Marks (70)
1	1714331001	ABHISHEK PATEL	12	13	47
2	1714331002	ADARSH KUMAR JHA	12	20	55
3	1714331003	AKSHANSH SINGH	14	AB	35
4	1714331004	AMAN KANSAL	12	3	36
5	1714331005	AMAN SINGH ASWAL	13	AB	41
6	1714331006	AMAN DESHWAL	12	AB	23
7	1714331007	AMIT YADAV	12	3	39
8	1714331008	ANJU SINGH	12	AB	30
9	1714331009	ANMOL LATIYAN	7	AB	7
10	1714331010	ANOOP KUMAR MISHRA	8	AB	50
11	1714331011	ANUJ SINGH	8	10	33
12	1714331012	ANUSHK SRIVASTAV	19	AB	37
13	1714331013	ARIHANT JAIN	AB	AB	32
14	1714331014	ASHISH KUMAR DUBEY	15	24	55
15	1714331015	ATUL KUMAR	AB	AB	5
16	1714331016	AYUSH AWASTHI	12	16	35
17	1714331017	CHAKSHU PARASHAR	10	AB	18
18	1714331018	GAURAV THAPLIYAL	0	3	10
19	1714331019	HARSHIT TOMAR	13	AB	28
20	1714331020	HIMANSHU GANGWAR	5	AB	10
21	1714331021	JANMEJAY SINGH CHAUHAN	21	AB	35
22	1714331022	JAYDEEP AGARWAL	23	AB	67
23	1714331023	KARAN SHARMA	13	23	47
24	1714331024	KARTIK SINGHAL	2	2	22
25	1714331025	KM. SHIVANGI AGRAWAL	26	AB	56
26	1714331026	KRISHNA MURARI RAI	5	7	34
27	1714331027	KULDEEP SINGH	12	AB	37
28	1714331029	MEGHA VISHWAKARMA	21	AB	28
29	1714331030	MUDIT GARG	8	AB	40
30	1714331031	MUKUL SINGH SISODIA	4	10	25
31	1714331032	NEERAJ KUMAR	12	AB	33
32	1714331034	NISHI GUPTA	28	AB	48
33	1714331035	NITIN KUMAR YADAV	4	4	16
34	1714331038	PIYUSH KUMAR SINGH	18	AB	39
35	1714331075	YATI SHINGAL	28	23	65

Number of Students in Section	35	35	35
Number of Students Present	33	14	35
No. of Students below 40%	11	8	9
Pass % (≥40%)	66.67%	42.85%	74.29%
Average Marks	12.43	11.5	34.8
Highest Marks Obtained	28	24	67

(Subject Teacher)
Mr. Praveen Kumar

(HoD/ECE)
Prof. (Dr.) R.P.S Chauhan 02/12/19

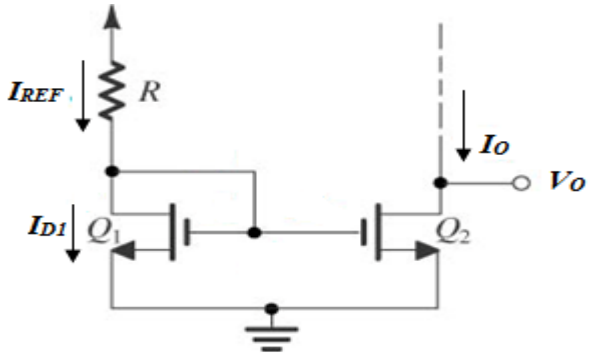
Subject Name : Integrated Circuits	Subject Code	REC-501
Date of Handout : 09-08-2019	Max Marks	
Date of Submission :14-08-2019		

ASSIGNMENT 1

Q.1. Explain MOSFET current mirror, also show the effect of V_o on I_o.

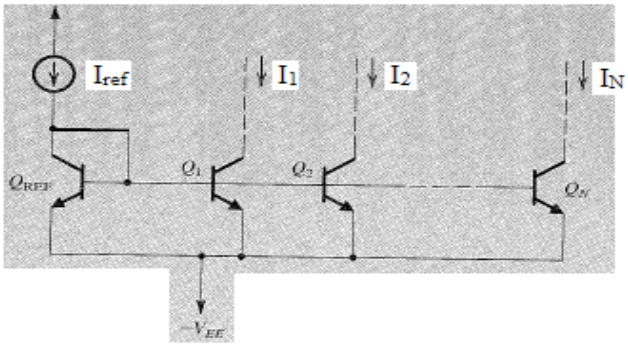
Q.2. Describe BJT current mirror and show the effect of finite β on the Current transfer ratio.

Q.3. For V_{dd} = 1.8V and using I_{REF} = 50µA. It is required to design the circuit of following fig. to obtain an output current whose nominal value is 50µA. Find R if Q_1 and Q_2 are matched with channel lengths of 0.5µm, channel widths of 5µm, V_t = 0.5V and k_n' = 250µA/V^2.What is the lowest possible value of V_o? Assuming that for this process technology the early voltage V'_A = 20V/µm, find the output resistance of current source.



Q.4. Following Fig. shows an N output current mirror. Assuming that all transistors are matched and have finite β and ignoring the effect of finite output resistances, show that

$$I_1 = I_2 = \ldots I_N = \frac{Iref}{1+\frac{N+1}{\beta}}$$



For β = 100, find the maximum number of outputs for an error not exceeding 10%.

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Tutorials/ Assignments/ Quizzes	Issue Date: 1 May 2010
Prepared by: MR	Approved by: Director

Subject Name : IC	Subject Code	REC-501
Date of Handout : 16.08.2019	Max Marks	
Date of Submission : 23.08.2019		

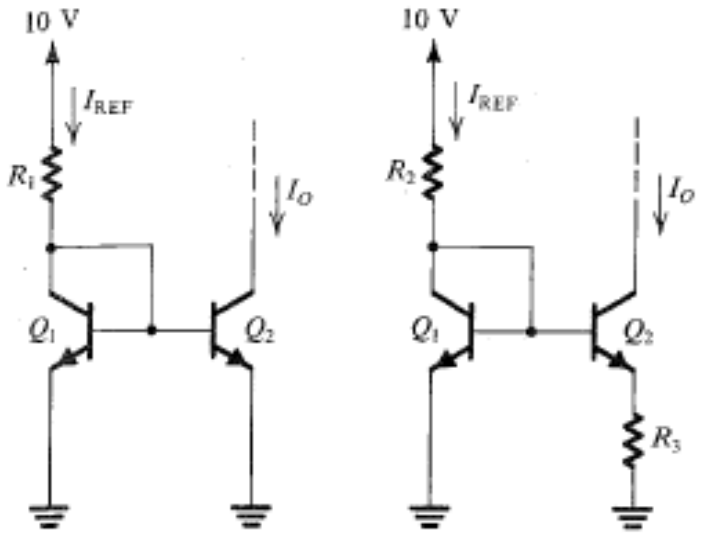
ASSIGNMENT 2

Q.1. Explain Wilson MOS mirror. Also draw the circuit of improved Wilson mirror.

Q.2. Draw the circuit of a bipolar mirror with base current compensation. Explain how it reduces the effect of β on current transfer ratio of current mirror.

Q.3. Explain the cascode current mirror. Write the advantage and disadvantage of the cascode current mirror.

Q.4. Explain Widlar current source.
Following figure (a) and (b) shows the two circuit for generating a constant current of 10μA which operates from 10V supply. Determine the value of required resistors assuming that V_{BE} = 0.7V at a current of 1mA and neglecting the effect of finite β.



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Tutorials/ Assignments/ Quizzes	Issue Date: 1 May 2010
Prepared by: MR	Approved by: Director

Subject Name : Integrated Circuits	Subject Code	REC-501
Date of Handout : 30-09-2019	Max Marks	
Date of Submission : 09-09-2019		

ASSIGNMENT 3

Q.1 Draw the circuit diagram of CMOS inverter and explain its transfer characteristics.

Q.2 List the advantage of CMOS logic family

Q.3 Draw the CMOS realization of the following Boolean expression

a) $Y = \overline{A + B(C + D}$ b) $Y = \overline{(A + B).C + D}$

c) $Y = \overline{A + (B + C) + D.E}$ d) $Y = AB + \bar{A}\bar{B}$ e) $Y = AB + C$

Q.4 Discuss the features of CMOS circuit. Realize one AND-OR-INVERT (AOI) and one OR- AND-INVERT (OAI) function using CMOS logic circuit.

Q.5 Design a CMOS full adder circuit with three inputs A, B, C and two output S and C_o.

Q.6 Give a CMOS logic circuit that realizes the function of three input odd parity checker. Specificially, the output is to be high when an odd number (1 or 3) of the input are high. Attempt a design with 10 transistors (not counting those in the inverters) in each of the PUN and PDN.

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Tutorials/ Assignments/ Quizzes	Issue Date: 1 May 2010
Prepared by: MR	Approved by: Director

Subject Name : Integrated Circuit	Subject Code	REC-501
Date of Handout : 13-09-2019	Max Marks	
Date of Submission : 19-09-2019		

ASSIGNMENT 4

Q.1 For a process technology with L=0.5µm, n=1.5, p=6. Give size of all transistors in (i) a four input NOR and (ii) a four input NAND Gate. Also compare the area of two Gates and then shows that CMOS NAND is preferred over CMOS NOR.

Q.2 Determine the W/L ratios for all transistor used in CMOS implementation of the function $Y = \overline{A(B + CD)}$

Q.3 Give the CMOS implementation of clocked SR flip-flop and explain its working.

Q.4 Draw the D-flip flop using CMOS. Also draw and explain its master slave configuration.

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Tutorials/ Assignments/ Quizzes	Issue Date: 1 May 2010
Prepared by: MR	Approved by: Director

Subject Name : Integrated Circuit	Subject Code	REC-501
Date of Handout : 27-09-2019	Max Marks	
Date of Submission : 03-10-2019		

ASSIGNMENT 5

Q.1 Define the following term with reference to op-amp
(i) CMRR (ii) Slew rate (iii) PSRR
(iv) Input offset voltage (v) Bias current

Q.2 Realize generalized impedance converter (GIC) with op-amp. How the inductor is simulated using this GIC.

Q.3 Draw a second order low-pass and high pass filter and drive its transfer function. Design a second order low pass butterworth filter having upper cut-off frequency of 1kHz and a passband gain of 2

Q.4 Derive the expression of voltage gain in KHN biquad filter.

Q.5 Draw the following Circuit using op-amp
(i) Weighted Summer (ii) Difference Amplifier
(iii) V-I converter (iv) I-V Converter

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Prepared by: MR	Approved by: Director

Subject Name : Integrated Circuit	Subject Code	REC-501
Date of Handout : 18-10-2019	Max Marks	
Date of Submission : 23-10-2019		

ASSIGNMENT 6

Q.1 Draw and explain the circuit of temperature compensated logarithmic amplifier.

Q.2 Draw and explain the circuit of temperature compensated anti-logarithmic amplifier.

Q.3 Draw and explain the circuit diagram of precision full wave rectifier.

Q.4 Explain inverting and non-inverting Schmitt trigger.

Q.4 Draw and explain the circuit of square wave generator circuit using op-amp.

IMS ENGINEERING COLLEGE	IMSEC/QF/48
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Tutorials/ Assignments/ Quizzes	Issue Date: 1 May 2010
Prepared by: MR	Approved by: Director

Subject Name : Integrated Circuit	Subject Code	REC-501
Date of Handout : 08-11-2019	Max Marks	
Date of Submission : 15-11-2019		

ASSIGNMENT 7

Q.1 Draw the functional block diagram of IC 555 and explain its working.

Q.2 Draw and explain monostable multivibrator using 555 timer and calculate its pulse width period.

Q.3 Draw and explain astable multivibrator using 555 timer and find the free running frequency of the output.

Q.4 An 8bit DAC has an input of 10011011 and 10V reference, find the corresponding output voltage.

Q.5 The basic step of a 8-bit DAC is 20mV. If 00000000 represents 0V, what is represented by the input 10110111.

Q.6 Explain the operation of Dual slope ADC.

(http://52.66.16.110/user)

- Dashboard (http://52.66.16.110/user#/dashboard)
- Module (http://52.66.16.110/user#/module_list)
- **Assignment**
  - Assignment
  - Student Wise Assignment Report
  - Faculty Wise Assignment Report
  - Section Wise Assignment Report

Assignment Report

Course	B.Tech	Stream	Electronics & Communication
Year	3 Year	Subject	Integrated Circuits (KEC 501)
Section	EC1		

#	Registered	Batch	Status	Roll No	Student Name	Assignment 07	Assignment 06	Assignment 05	Assignment 04	Assignment 03	Assignment 02	Assignment 01	Total
1	Yes	EC1	Regular	1714331042	RAHUL SINGH	1	0	1	1	1	1	1	6
2	Yes	EC1	Regular	1814331002	AASHI SINGH	1	1	0	1	1	1	1	6
3	Yes	EC1	Regular	1814331003	ABHISHEK KUMAR	1	1	1	1	1	1	1	7
4	Yes	EC1	Regular	1814331004	ABHISHEK KANDPAL	1	1	1	1	1	1	1	7
5	Yes	EC1	Regular	1814331005	ADITYA KUMAR	1	1	1	1	1	1	0	6
6	Yes	EC1	Regular	1814331006	ADITYA PANDEY	1	1	1	1	1	1	1	7
7	Yes	EC1	Regular	1814331007	AKHIL RUHELA	1	1	1	1	1	1	1	7
8	Yes	EC1	Regular	1814331008	AKSHAY VERMA	1	1	1	0	1	1	1	6
9	Yes	EC1	Regular	1814331009	ALI MAJAZ	1	1	1	1	1	1	1	7
10	Yes	EC1	Regular	1814331010	AMAN SAIFI	1	1	1	1	1	1	1	7
11	Yes	EC1	Regular	1814331011	ANIRUDH MANOJ	0	0	0	1	1	1	1	4
12	Yes	EC1	Regular	1814331012	ANMOL SHARMA	1	1	1	1	1	1	1	7
13	Yes	EC1	Regular	1814331013	ANSHUL SHARMA	1	1	1	1	1	1	1	7
14	Yes	EC1	Regular	1814331014	ANTRIKSH SAXENA	1	1	1	1	1	1	1	7
15	Yes	EC1	Regular	1814331015	ANUBHAV SINGH	1	1	1	1	1	1	1	7
16	Yes	EC1	Regular	1814331016	ARBAZ AKHTAR	1	1	1	1	1	1	1	7
17	Yes	EC1	Regular	1814331017	ARPIT SONI	1	1	1	1	1	1	1	7
18	Yes	EC1	Regular	1814331018	ASHISH CHAUDHARY	1	1	0	1	1	1	1	6
19	Yes	EC1	Regular	1814331019	ASHISH SHARMA	1	1	1	1	1	1	1	7
20	Yes	EC1	Regular	1814331020	AYUSH SAINI	0	1	0	0	1	1	1	4
21	Yes	EC1	Regular	1814331021	HARDIK RASTOGI	1	1	1	1	1	1	1	7
22	Yes	EC1	Regular	1814331022	HARSH JAISWAL	1	1	1	1	1	1	1	7
23	Yes	EC1	Regular	1814331023	JATIN AGARWAL	1	1	1	1	1	1	1	7
24	Yes	EC1	Regular	1814331024	JATIN RANA	1	1	1	1	1	1	1	7

(http://52.66.16.110/user)

Dashboard (http://52.66.16.110/user#/dashboard)

Module (http://52.66.16.110/user#/module_list)

Assignment

Assignment

Student Wise Assignment Report

Faculty Wise Assignment Report

Section Wise Assignment Report

#	Registered	Batch	Status	Roll No	Student Name	Assignment 07	Assignment 06	Assignment 05	Assignment 04	Assignment 03	Assignment 02	Assignment 01	Total
25	Yes	EC1	Regular	1814331025	JAYA SINHA	1	1	1	1	1	1	1	7
26	Yes	EC1	Regular	1814331026	KRITIKA NATH	1	1	1	1	1	1	0	6
27	Yes	EC1	Regular	1814331027	MANSI SAXENA	1	1	1	1	1	1	1	7
28	Yes	EC1	Regular	1814331028	ARMAN SHAH	1	1	1	1	1	1	1	7
29	Yes	EC1	Regular	1814331029	MUDIT PRATAP SINGH	1	1	1	1	1	1	1	7
30	Yes	EC1	Regular	1814331030	MUKUL CHAUHAN	1	1	1	1	1	1	1	7
31	Yes	EC1	Regular	1814331031	MUNESH KUMAR SINGH	1	1	0	1	0	1	1	5
32	Yes	EC1	Regular	1814331032	MANIK CHOUDHARY	1	1	1	1	1	1	1	7
33	Yes	EC1	Regular	1814331033	NIKHIL KUMAR	0	1	1	1	1	1	1	6
34	Yes	EC1	Regular	1814331034	NISHA .	1	1	1	1	1	1	1	7
35	Yes	EC1	Regular	1814331035	NITESH UPADHYAY	1	1	1	1	1	1	1	7
36	Yes	EC1	Regular	1814331036	PRABHAT MITTAL	1	1	1	1	1	1	1	7
37	Yes	EC1	Regular	1814331037	PRADEEP DUBEY	1	1	1	1	1	1	1	7
38	Yes	EC1	Regular	1814331038	PRAKHAR TRIVEDI	1	0	0	0	1	1	0	3
39	Yes	EC1	Regular	1814331039	RACHIT GARG	1	1	1	1	1	1	1	7
40	Yes	EC1	Regular	1814331040	RISHABH GUPTA	1	0	1	1	1	1	1	6
41	Yes	EC1	Regular	1814331041	RIYA AGARWAL	1	1	1	1	1	1	1	7
42	Yes	EC1	Regular	1814331042	SAKSHI VARSHNEY	1	1	1	1	1	1	1	7
43	Yes	EC1	Regular	1814331043	SARANSH RAI	1	1	1	1	1	1	1	7
44	Yes	EC1	Regular	1814331044	SARTHAK GUPTA	1	1	1	1	1	1	1	7
45	Yes	EC1	Regular	1814331045	SAURABH GUPTA	1	1	1	1	1	1	1	7
46	Yes	EC1	Regular	1814331046	SHASHWAT DWIVEDI	0	1	1	1	1	1	1	6
47	Yes	EC1	Regular	1814331047	SHELENDRA RAGHAV	1	0	0	0	1	1	0	3
48	Yes	EC1	Regular	1814331048	SHIVAM KATIYAR	1	1	1	1	1	1	1	7
49	Yes	EC1	Regular	1814331049	SHIVANGI MISHRA	1	1	1	1	1	1	1	7
50	Yes	EC1	Regular	1814331050	SUPREET DEOL	1	1	1	1	1	1	1	7
51	Yes	EC1	Regular	1814331051	TANISH VARSHNEY	1	1	1	1	1	1	1	7
52	Yes	EC1	Regular	1814331052	TANISHKA VATS	1	1	1	1	1	1	1	7
53	Yes	EC1	Regular	1814331053	TUSHAR KUMAR	1	1	1	1	1	1	1	7
54	Yes	EC1	Regular	1814331054	UTKARSH SINGH	0	1	1	1	1	1	1	6
55	Yes	EC1	Regular	1814331055	VED PRAKASH SHARMA	1	1	1	1	1	1	1	7
56	Yes	EC1	Regular	1814331056	VISHAL RANA	1	1	1	1	1	1	1	7

(http://52.66.16.110/user)

- Dashboard (http://52.66.16.110/user#/dashboard)
- Module (http://52.66.16.110/user#/module_list)
- **Assignment**
  - Assignment
  - Student Wise Assignment Report
  - Faculty Wise Assignment Report
  - Section Wise Assignment Report

#	Registered	Batch	Status	Roll No	Student Name	Assignment 07	Assignment 06	Assignment 05	Assignment 04	Assignment 03	Assignment 02	Assignment 01	Total
57	Yes	EC1	Regular	1814331057	YASH DIXIT	1	1	0	0	0	0	0	2
58	Yes	EC1	Regular	1814331058	YASHASVI SINGH	1	1	1	1	1	1	1	7

IMS Engineering College Ghaziabad

Department of Electronics & Communication Engineering

* Required

1. Email address *

Quiz

Subject Name :-Digital System Design

Subject Code :- KEC 302

2. Roll No. *

3. Name *

Important Instructions

1. All questions are compulsory. Each question carry one mark.
2. You are allowed to submit only once, therefore verify your answers before submission.
3. Do not submit using multiple email ids, this may lead to cancellation of your exam.

4. A D flip flop can be constructed from which flip flop by using an additional NOT gate. * 1 point

Mark only one oval.

- S-R
- Both J-K and S-R
- J-K
- T

5. Determine the characteristic equation of T flip flop? * 1 point

Mark only one oval.

- Qn+1=Tn.Qn' + Tn'.Qn
- Qn+1=Tn.Qn + Tn'.Qn
- Qn+1=Tn.Qn + Tn'.Qn'
- Qn+1=Tn + Tn'.Qn

6. Which of the following flip flop is not free from race around condition? * 1 point

Mark only one oval.

- D Flip Flop
- T Flip Flop
- JK Flip Flop
- Master Slave JK Flip Flop

7. Question * 1 point

Consider the following state table:

Present state	Next state		Output	
	X = 0	X = 1	X = 0	X=1
a	a	b	0	1
b	c	d	0	0
c	a	d	0	1
d	e	f	1	0
e	a	f	1	0
f	g	f	1	0
g	a	f	1	0

Which of the following statements are TRUE?

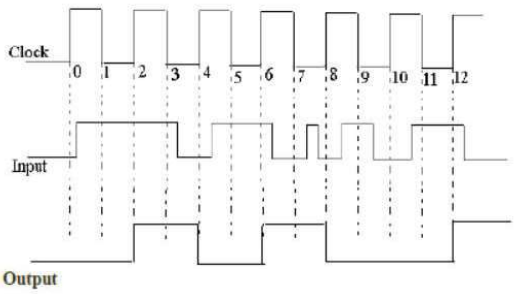
I. The state table corresponds to a Mealy Machine.
II. The number of states can be reduced to a minimum of 5 states.
III. The number of states can be reduced to a minimum of 6 states.
IV. States 'd', 'e', 'f' and 'g' are equivalent.
V. States 'd' and 'f' are equivalent.

Mark only one oval.

- III, IV, V only
- I, III, IV only
- I, II, V only
- II, IV, V only

8. Question * 1 point

The waveform indicates the operation of

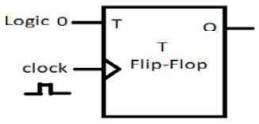


Mark only one oval.

- Negative edge triggered J-K Flip Flop
- Positive edge triggered S-R Flip Flop
- Positive edge triggered D Flip Flop
- Negative edge triggered T Flip Flop

9. * 1 point

What is the output frequency of the following circuit for 5MHz clock signal?
(Assume initial values of Q is logic 1)

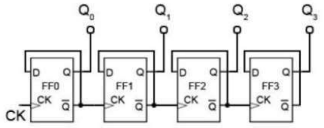


Mark only one oval.

- 5 MHz
- 0 MHz
- 10 MHz
- 2.5 MHz

10. Question * 1 point

Identify the outputs of the following circuit after five clock transitions. The initial values of all flip-flops are 0.

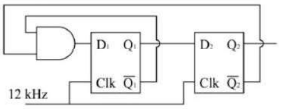


Mark only one oval.

- Q3 Q2 Q1 Q0 = 0101
- Q3 Q2 Q1 Q0 = 0000
- Q3 Q2 Q1 Q0 = 0011
- Q3 Q2 Q1 Q0 = 1100

11. Question * 1 point

In the circuit shown, the clock frequency, i.e., the frequency of the Clk signal, is 12 kHz. The frequency of the signal at Q2 is _____ kHz.

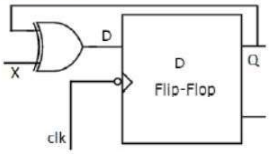


Mark only one oval.

- 12 kHz
- 3 kHz
- 4 kHz
- 36 kHz

12. Question * 1 point

Identify the operation of following circuit.



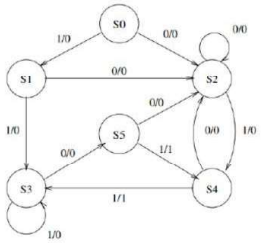
Mark only one oval.

- D Flip Flop
- T Flip Flop
- SR Flip Flop
- JK Flip Flop

13. Question * 1 point

Let X is the input sequence whereas Z is the output sequence for the state machine shown below. Which of the following options correctly describes the output Z sequence for input sequence X given below (Assume initial state S0)

X = 1 0 1 1 0 0 1



Mark only one oval.

- Z = 1011001
- Z = 0100110
- Z = 0001000
- Z= 0000100

14. CMOS is not preferred for * 1 point

Mark only one oval.

- Low power dissipation
- Small size
- Good immunity to noise
- High switching speed

15. Which of the following has the highest noise margin * 1 point

Mark only one oval.

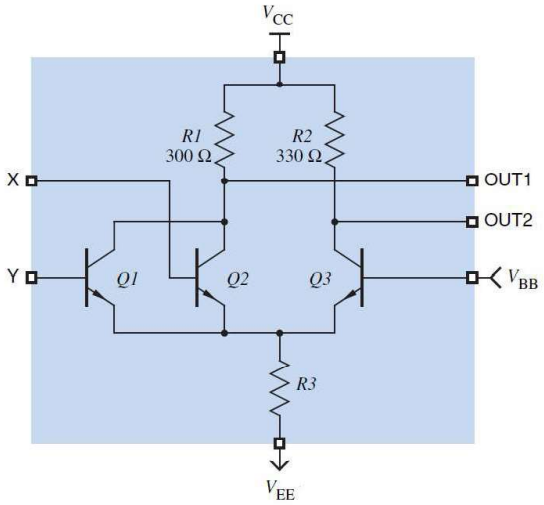
- TTL
- RTL
- ECL

16. Which of the following has highest speed * 1 point

Mark only one oval.

- TTL
- CML
- CMOS
- RTL

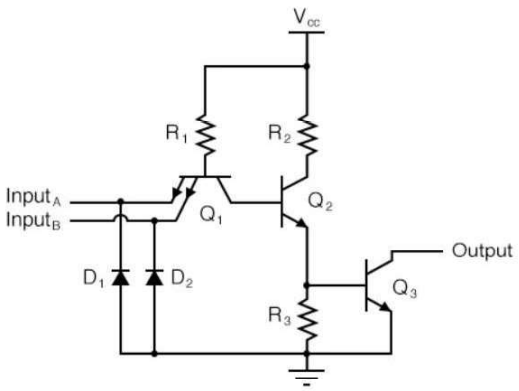
17. The following is a circuit of * 1 point



Mark only one oval.

- RTL NOR/OR gate
- TTL NOR/OR gate
- ECL NOR/OR gate
- CMOS NOR/OR gate

18. The following is a circuit of * 1 point



Mark only one oval.

- RTL NOR gate
- TTL NAND Gate
- ECL NOR/OR gate
- RTL NAND gate
- TTL NOR gate

Dashboard
Module
Academic
Notice
Schedule
Attendence Reports
Test Marks
Feedback
Complaint
Grade Result
Gate Pass List

Student Feedback

B.Tech - Electronics & Communication - 2 Year - EC1

Faculty Name	Subject Code	Subject Name	Subject knowledge and lecture delivery	Generates interest in the subject	Encourages questions from students	Maintains class discipline	Supplements lectures with PPT/Video lesson/Quiz	Links subject with life experiences	Total Marks	Status
Neeraj Jain	KEC 403	Signals & Systems	36.77	12.59	12.84	8.78	4.34	8.61	83.93	Very Good
Mayurika Saxena	KOE 044	SENSOR AND INSTRUMENTATION	41.49	13.92	13.92	9.06	4.34	9.06	91.79	Excellent
Suman Gupta	KVE-401	UNIVERSAL _HUMAN_VALUES	38.75	12.66	13.08	7.94	4.14	9.22	85.79	Very Good
R N Baral	KEC 401	COMMUNICATION ENGINEERING	40.23	13.08	12.92	8.56	4.25	8.44	87.48	Very Good
Praveen Kumar	KEC 402	ANALOGCIRCUIT	41.49	13.25	13.59	9.06	4.31	8.39	90.09	Excellent

→ Sujeet Kumar
ECE Deptt.

Faculty Feedback 2015-2016 (1)(Even Semester)

Faculty Name	Subject Code	Year	Branch	Lect Delivery average	Subject Understanding average	Punctuality average	Timely Assig given average	Timely Assig check average	AVERAGE	Status
Mr. Sujeet Kumar	NEC-603	3	2EC	76.77	78.71	90.32	91.61	89.68	85.42	Very Good
Mr. Sujeet Kumar	EOE-081	4	2EC	87.37	81.75	86.67	88.77	88.77	86.67	Very Good

Faculty Feedback 2015-2016 (1)(Odd Semester)

Faculty Name	Subject Code	Year	Branch	Lect Delivery average	Subject Understanding average	Punctuality average	Timely Assig given average	Timely Assig check average	AVERAGE	Status
Mr. Sujeet Kumar	NEC-302	2	2EC	2.7948718	2.7948718	3	2.5128205	2.6153846	2.7435896	Good
Mr. Sujeet Kumar	EEC-703	4	2EC	4.0526314	3.9210527	4.2105265	4.2105265	4.3157897	4.142105	Excellent

Faculty Feedback 2014-2015 (1)(Even Semester)

Faculty Name	Subject Code	Year	Branch	Lect Delivery Percentage	Subject Understanding Percentage	Punctuality Percentage	Timely Assig given Percentage	Timely Assig check Percentage	Percentage	Status
Mr. Sujeet Kumar	EEC-601	3	2EC	91.43	85.71	85.71	100	100	92.57	Excellent

Sujeet Kr
23/9/16

Faculty Name - Praveen kumar

Faculty Feedback 2015-2016 (1)(Even Semester)										
Faculty Name	**Subject Code**	**Year**	**Branch**	**Lect Delivery average**	**Subject Understanding average**	**Punctuality average**	**Timely Assig given average**	**Timely Assig check average**	**AVERAGE**	**Status**
Mr. Praveen Kumar	EEC-035	4	EC2	85.66	84.53	84.91	86.42	81.89	84.68	Very Good
Mr. Praveen Kumar	NEC-603	3	EC1	95.45	93.64	94.55	95.91	94.55	94.82	Excellent

Faculty Feedback 2015-2016 (1)(Odd Semester)										
Faculty Name	**Subject Code**	**Year**	**Branch**	**Lect Delivery average**	**Subject Understanding average**	**Punctuality average**	**Timely Assig given average**	**Timely Assig check average**	**AVERAGE**	**Status**
Mr. Praveen Kumar	NEC-501	3	EC1	4.037037	4.037037	4.037037	3.6666667	3.7037036	3.8962963	Very Good
Mr. Praveen Kumar	NIC-501	3	2EC	4.423077	4.3846154	4.3461537	4.3846154	4.1923075	4.3461537	Excellent

IMS ENGINEERING COLLEGE, GHAZIABAD

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MONTHLY REPORT

Syllabus covered and assignment report

Date: 19-03-15
Year/ semester: EC2 4th yr
Section: EC1/EC2/2EC
Name of coordinator: Praveen kumar

Subject code	Subject name	Faculty name	Unit covered(%) /total unit	no of assignment	No. of lectures proposed/ held	signature
EEC 801	Mobile & Wireless Comm.	Abhishek Sharma	2.0	3 (Three)	26	Abhishek
EEC035	Intro. to Radar Systems	Praveen kr	2.0	3	31	kumar
EOE081	NCER	Mukesh Khandelwal	2.0	2	33	
EEC 802	Electronics switching	T.N. Vashisth	2.6	4	30	

kumar
(Praveen kumar)
Signature
Year coordinator

IMS ENGINEERING COLLEGE, GHAZIABAD

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

MONTHLY REPORT

Syllabus covered and assignment report

Date:

Year/ semester: 2nd year/ 4th semester

Section: EC1/EC2/2EC

Name of coordinator: Akanksha Shukla

Subject code	Subject name	Faculty name	Unit covered(%)/total unit	no of assignment	No. of lectures proposed/ held	signature
NEC-402	Electronic circuits	Praveen kumar	47%	4	38	
NEC-408	Electronic measurement and instrumentation	Akashdeep	45%	4	22	
NEC-404	EMFT	Manish Zadoo	40%	4	35	
NAS-401	Engg. Mathematics-III	Solabh	40%	4	36	
NEC-401	Data structure	Kirti	40%	2	30	Kirti
NHU-402	Industrial Psychology	Akanksha Shukla	40%	4	19	
AUC-001	Human Values & Professional Ethics	Ankita Bhardwaj	40%	4	06	

Ashukla EC-1

(Akanksha Shukla)

Signature

Year coordinator